

PG142-B00

DP + DP + DP + HDMI/DP

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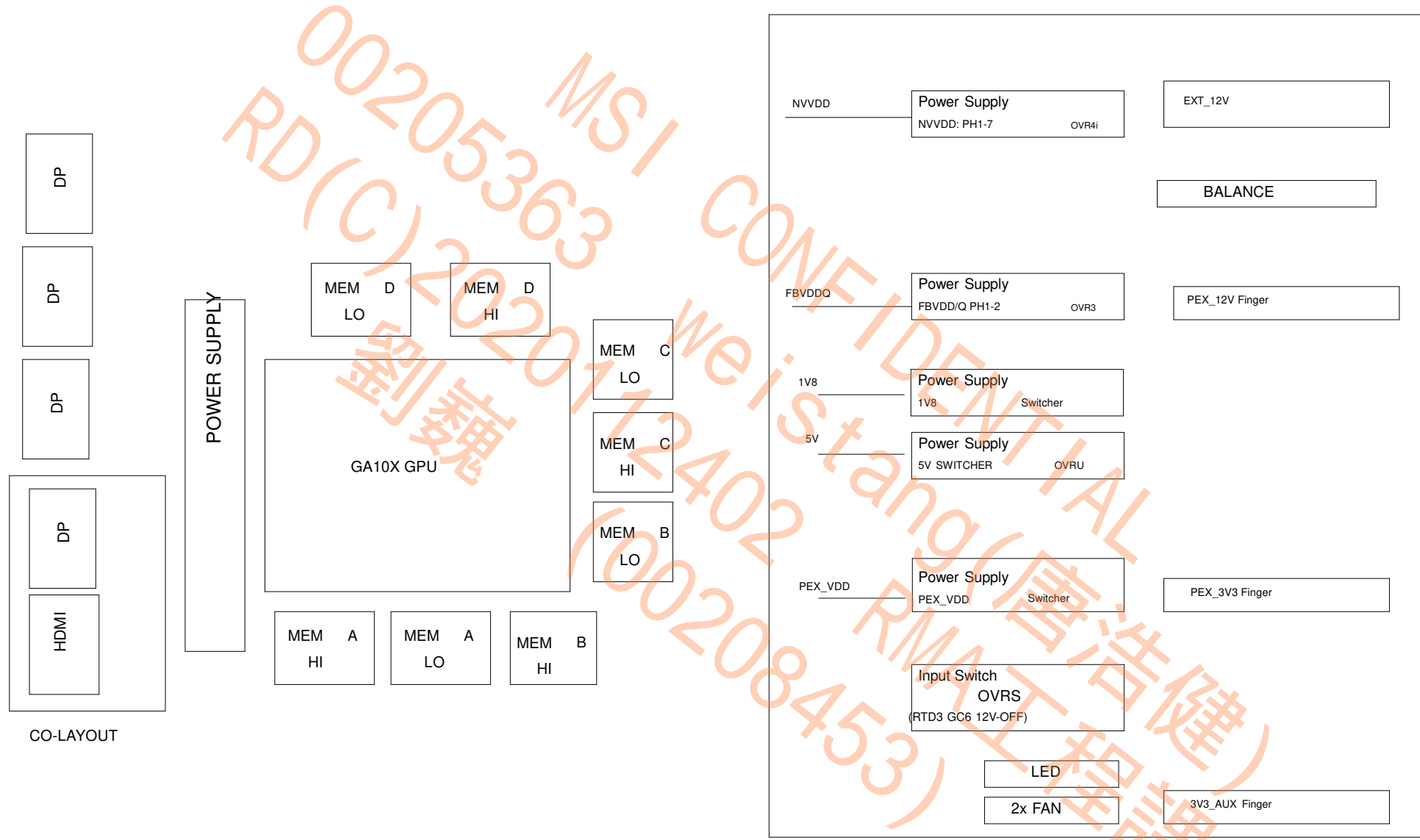
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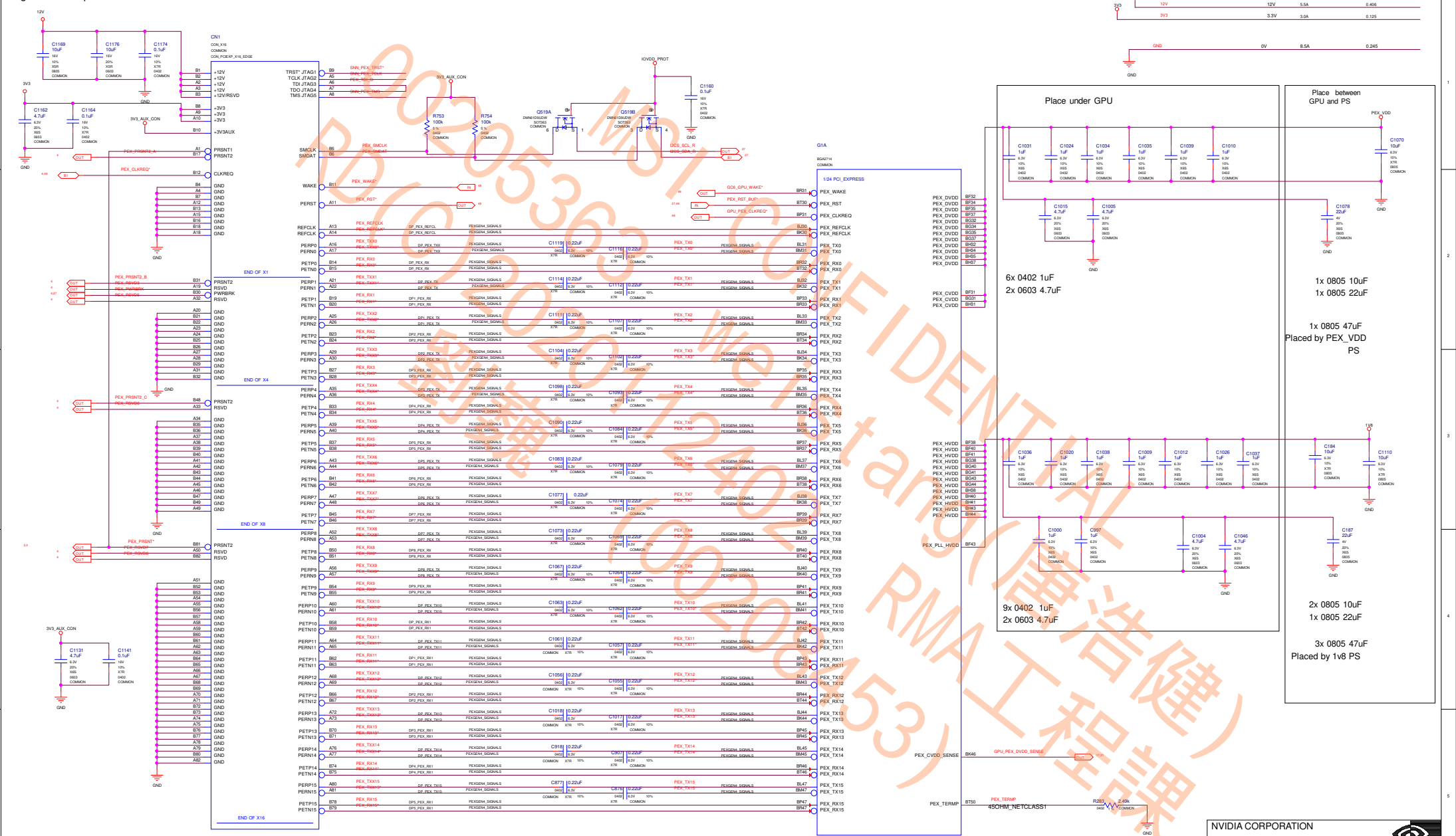
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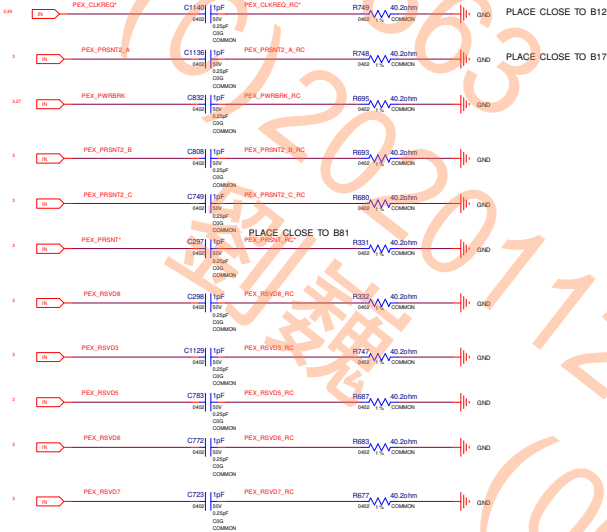


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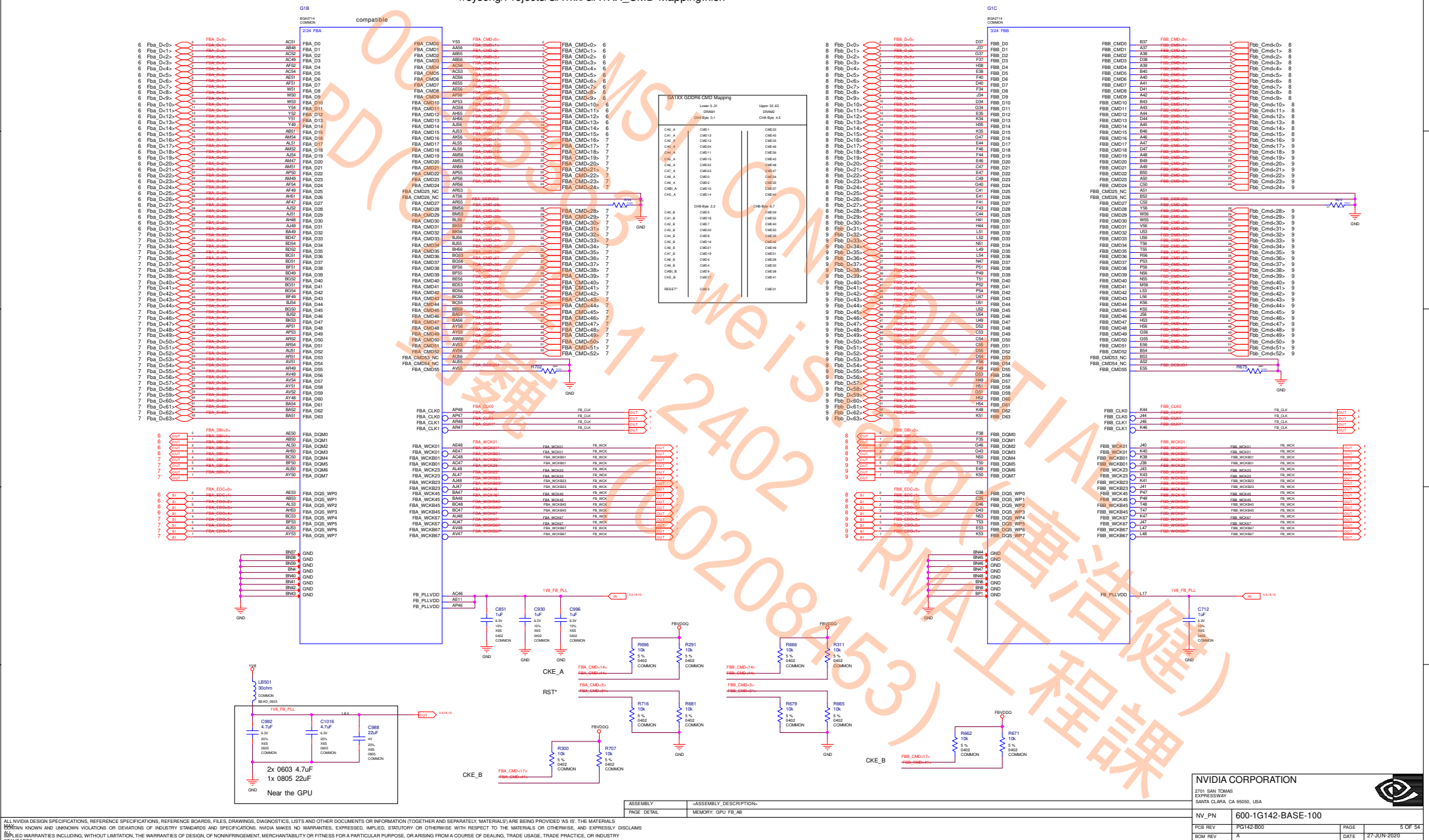
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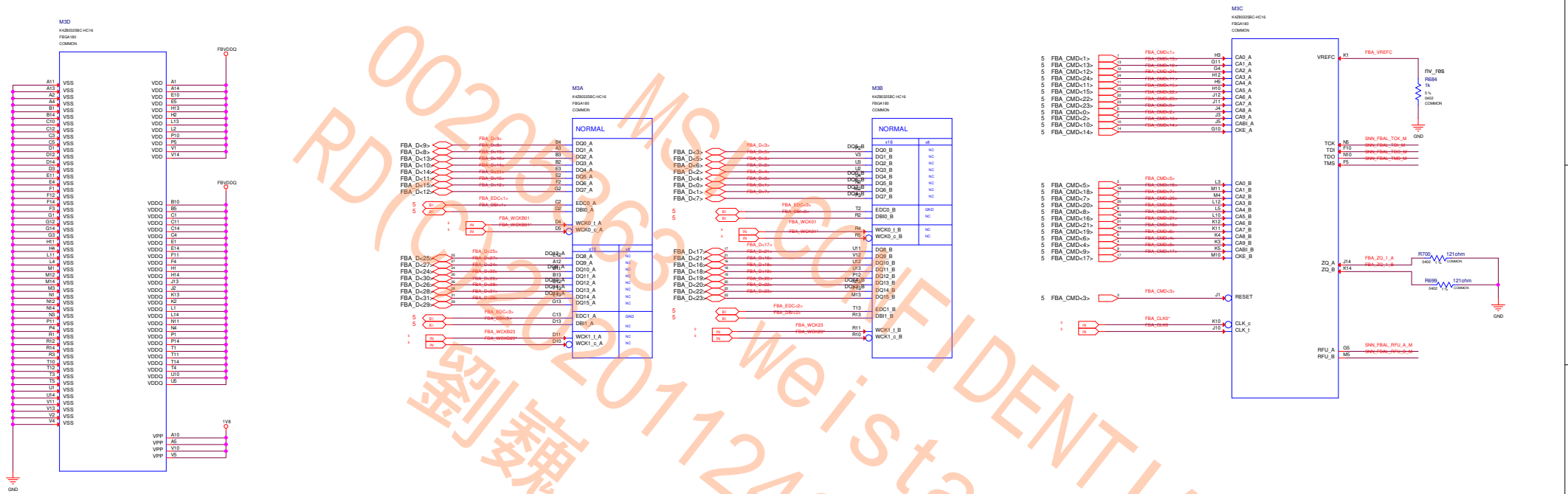
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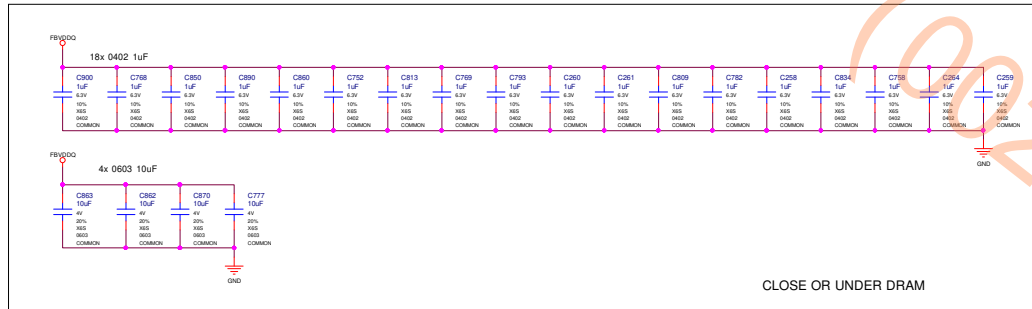


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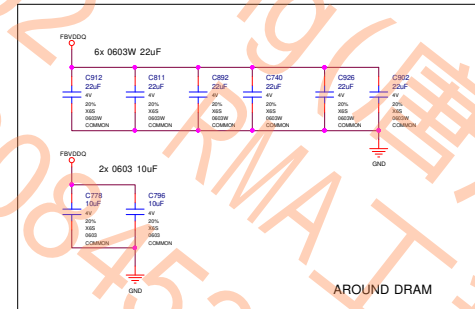
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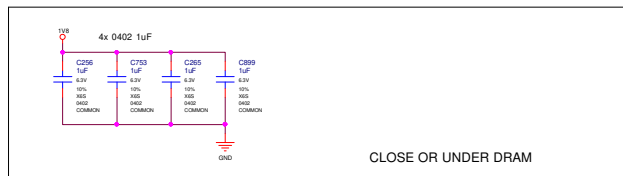
decap via : at least 2 grnd vias and 2 power vias for each cap



CLOSE OR UNDER DRAM



AROUND DRAM



CLOSE OR UNDER DRAM

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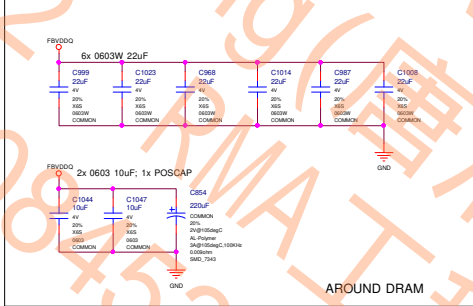
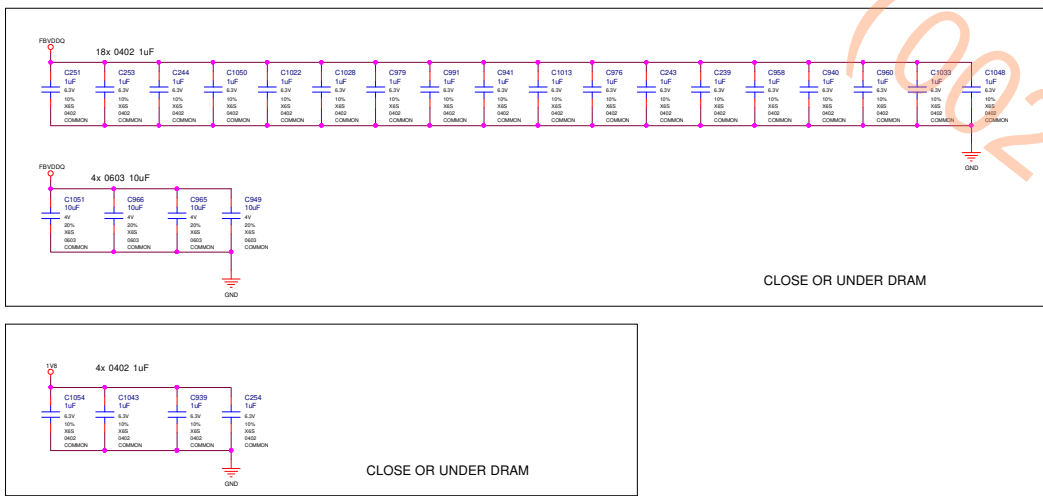
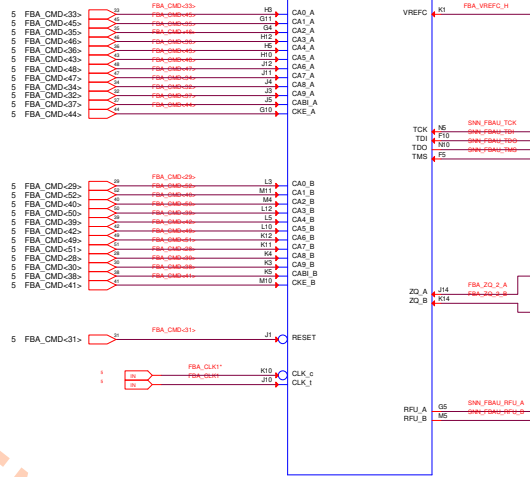
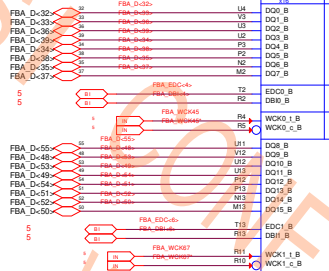
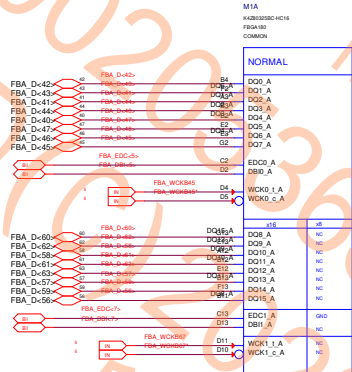
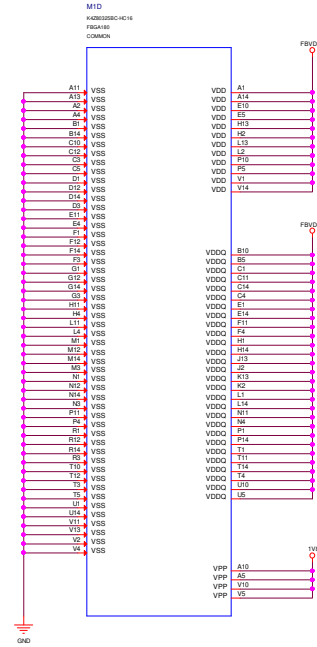
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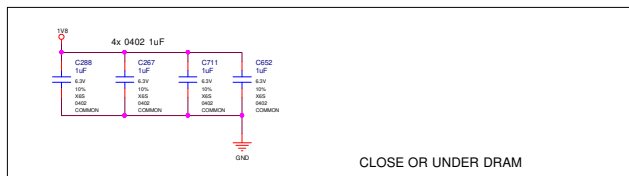
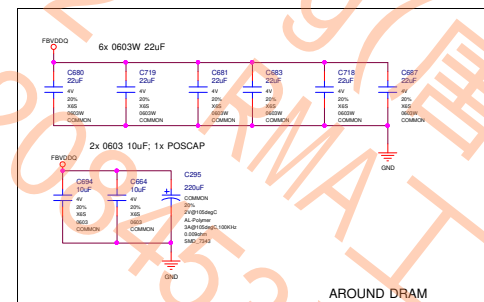
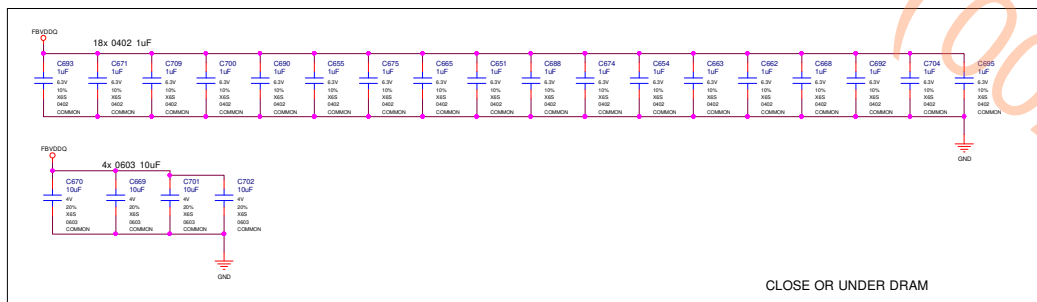
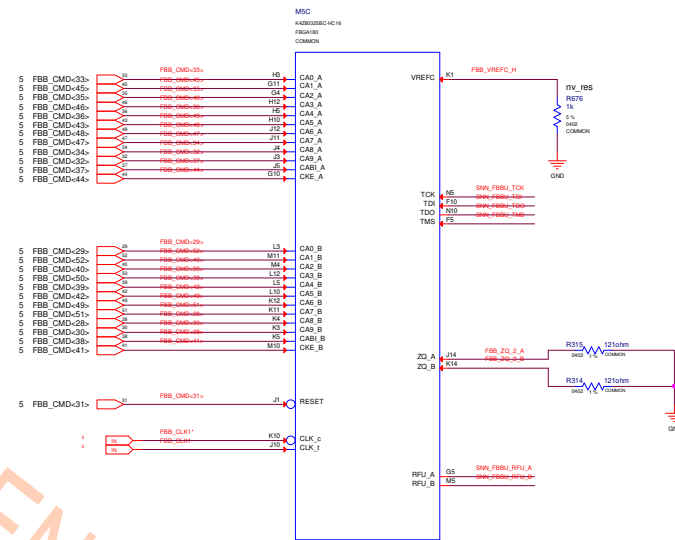
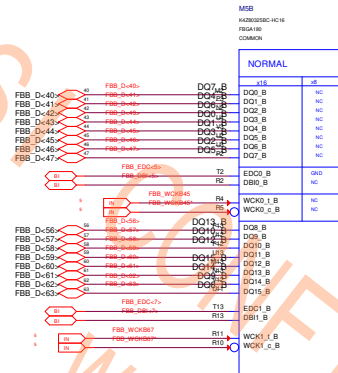
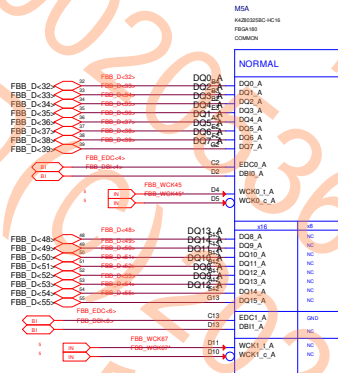
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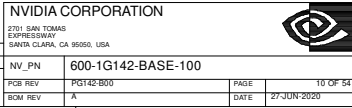
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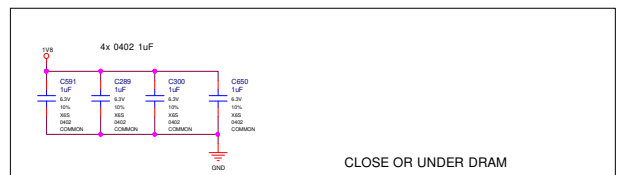
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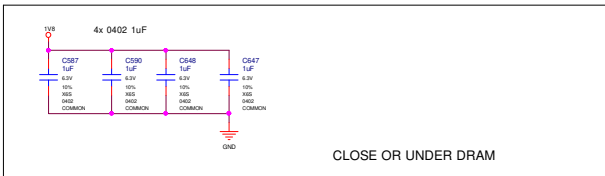
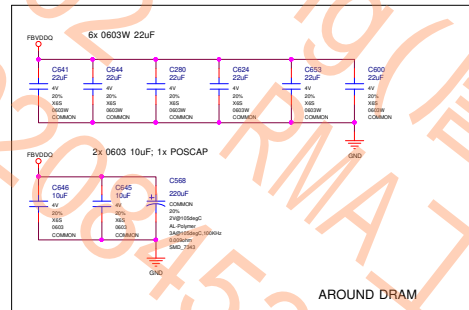
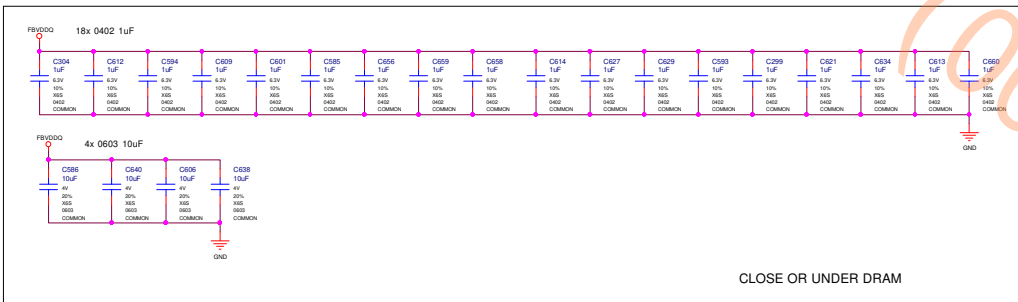
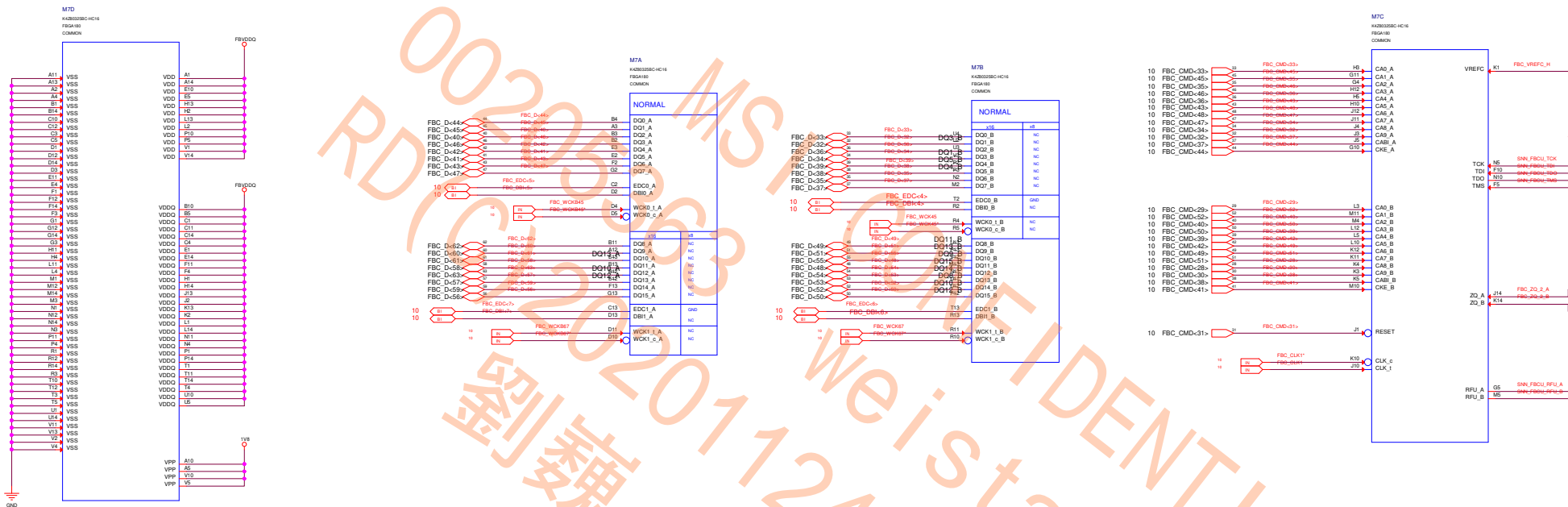




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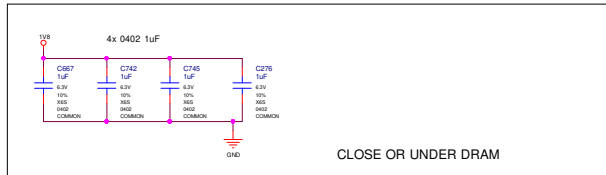
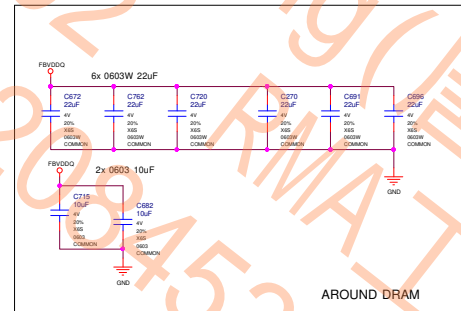
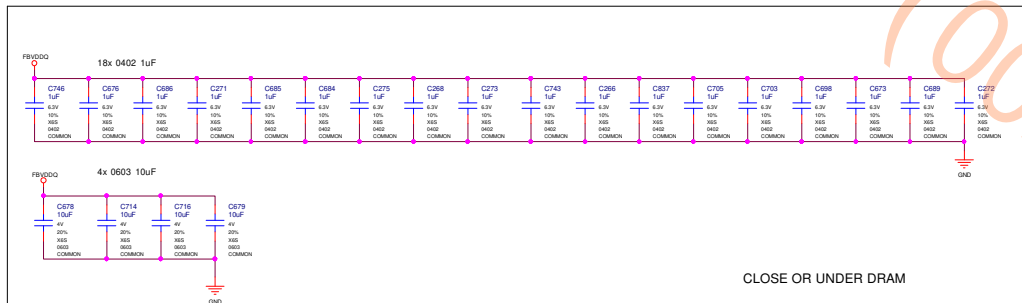
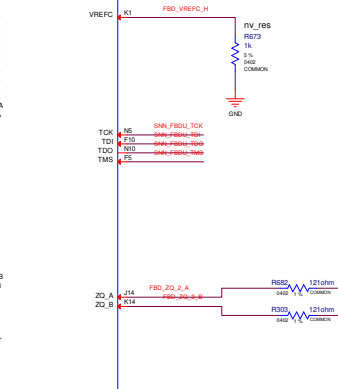
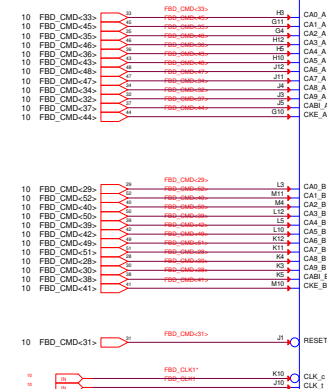
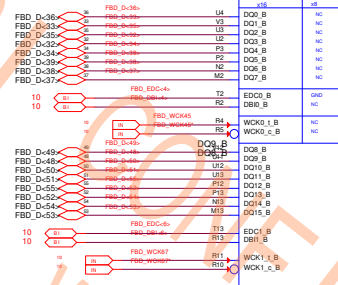
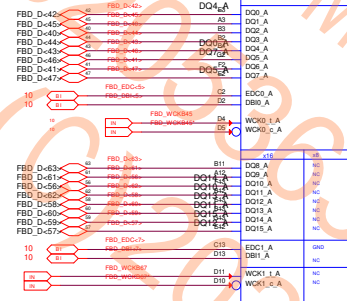
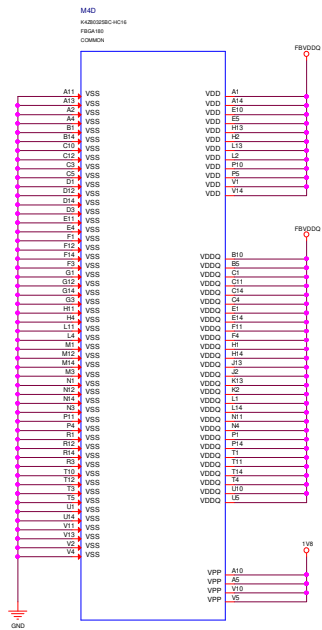
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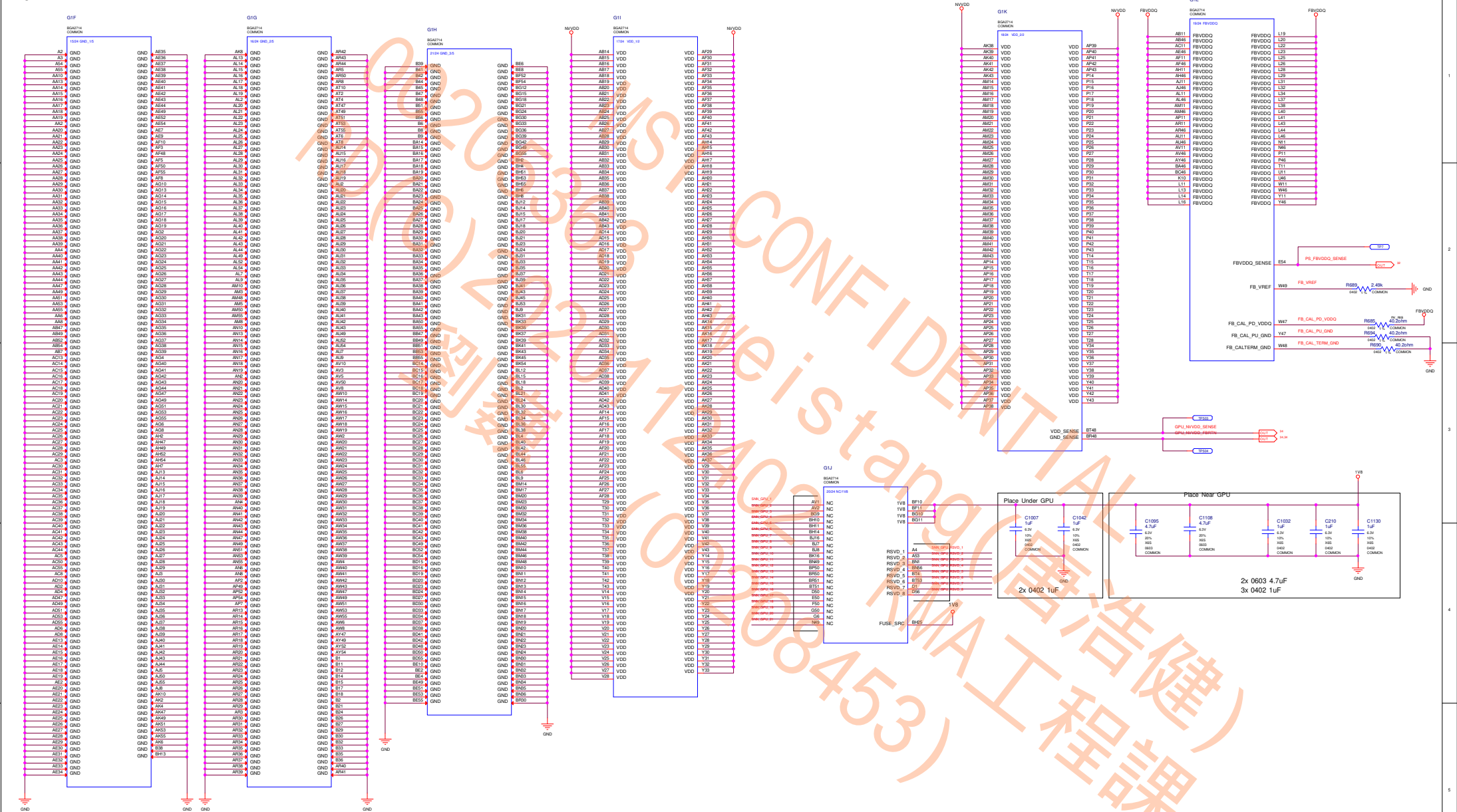


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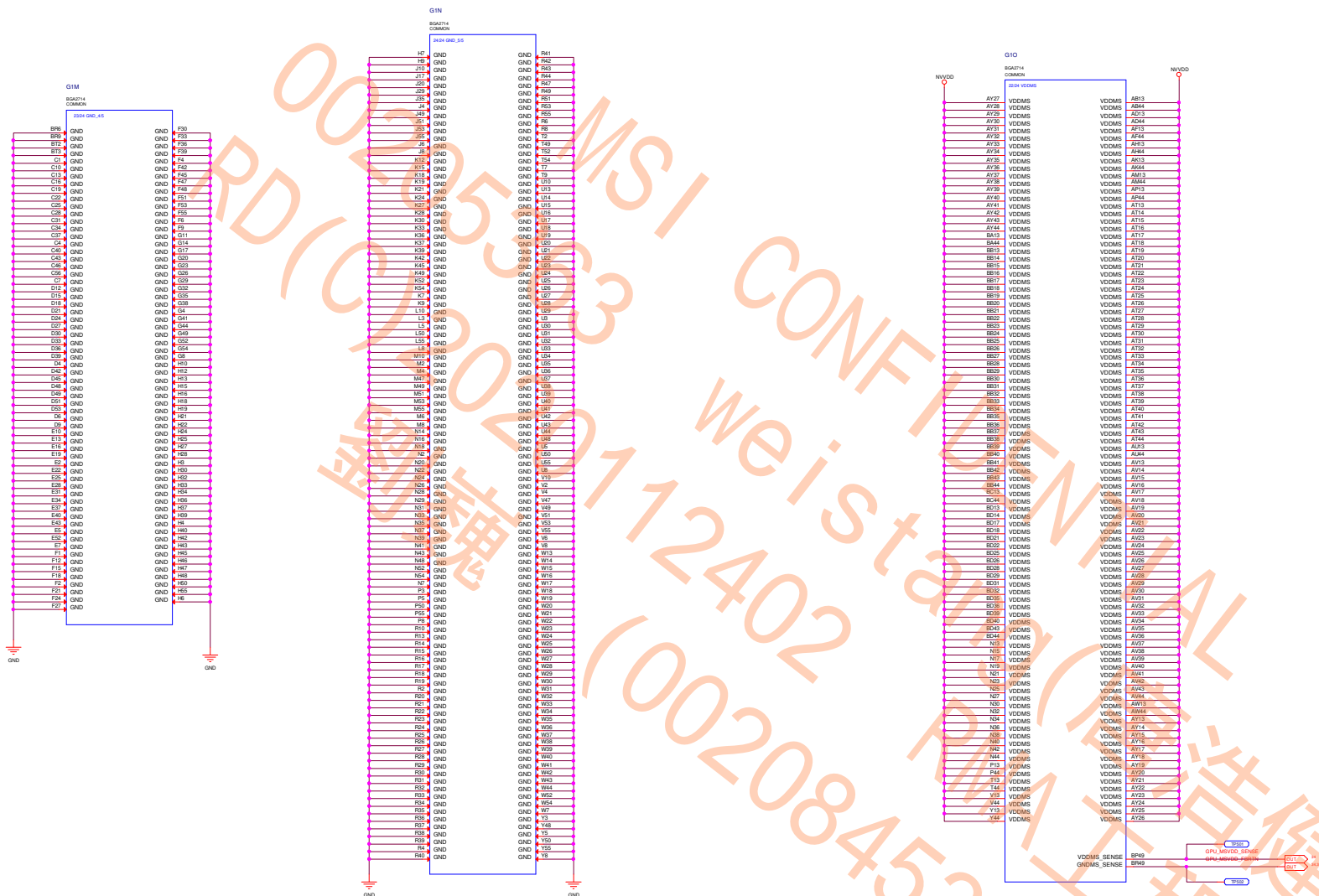
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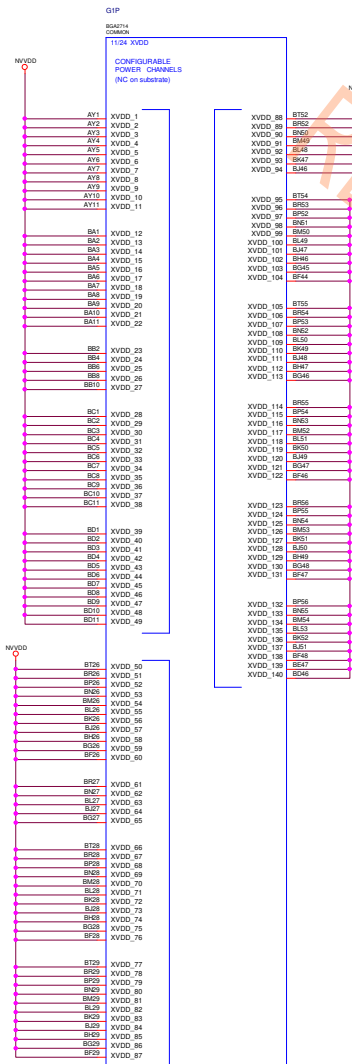
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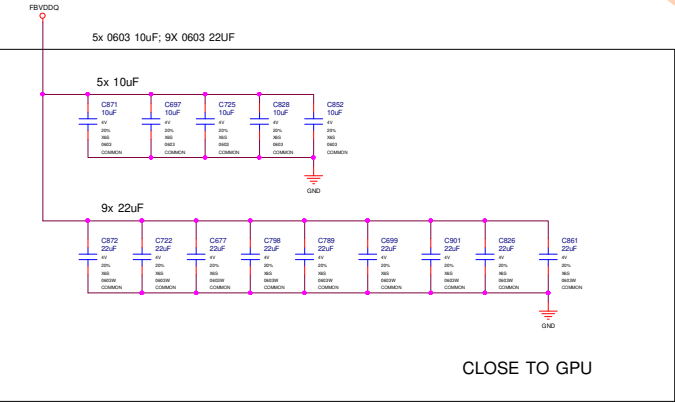
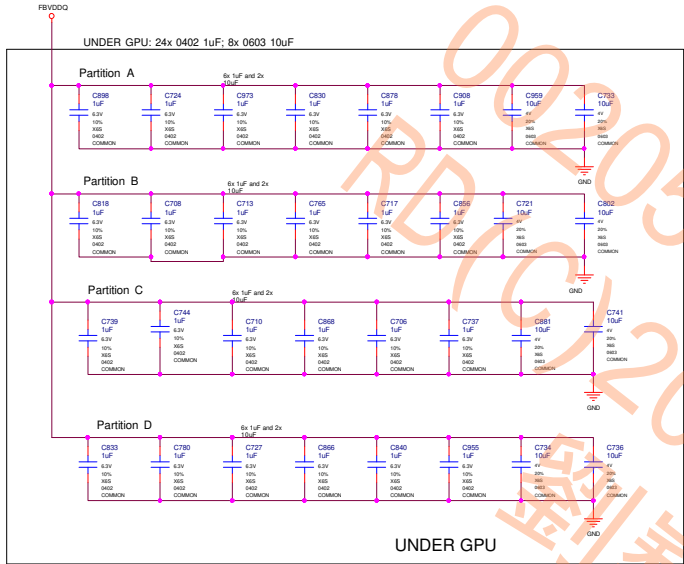


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ASSEMBLY	ASSEMBLY DESCRIPTION
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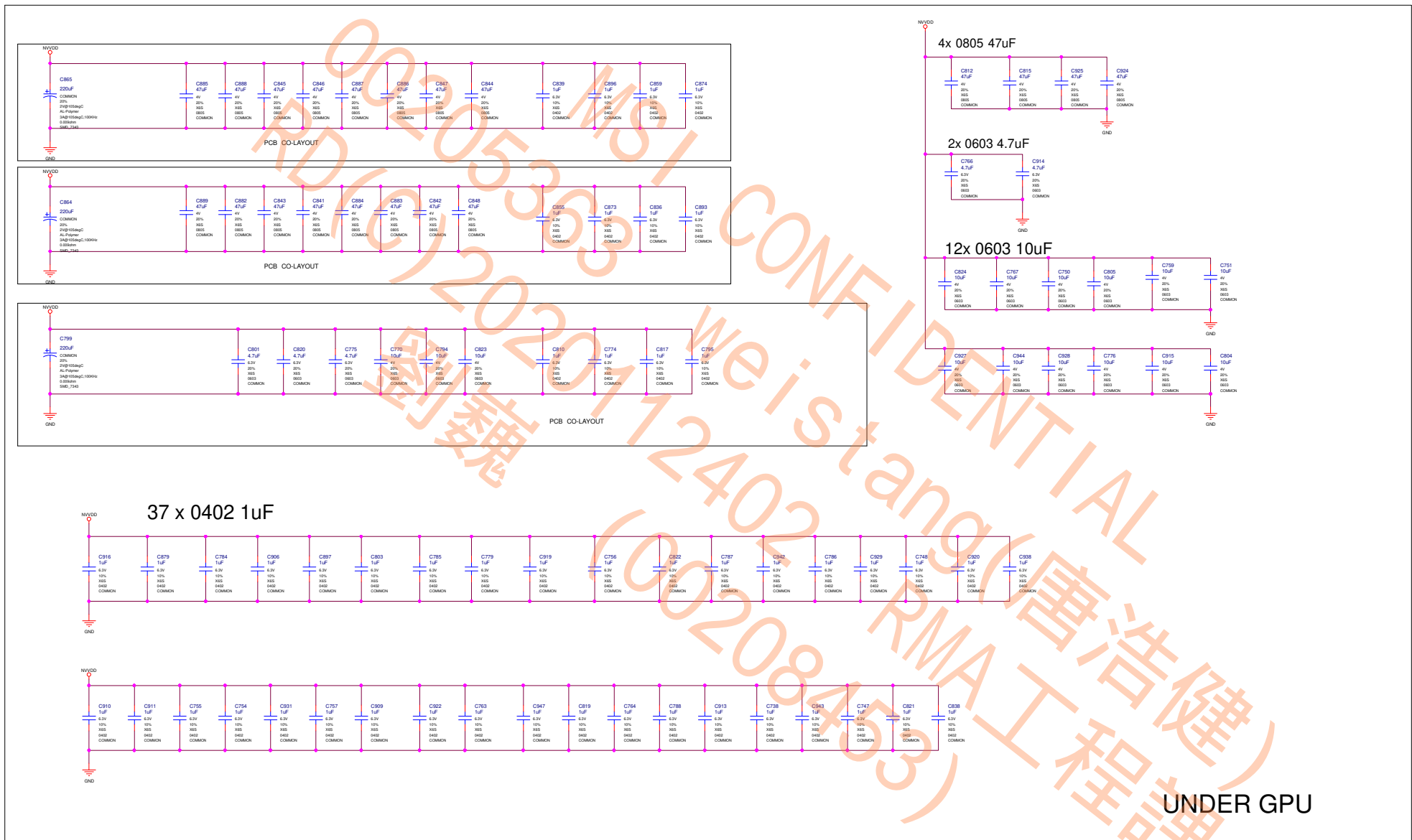
FBVDDQ



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
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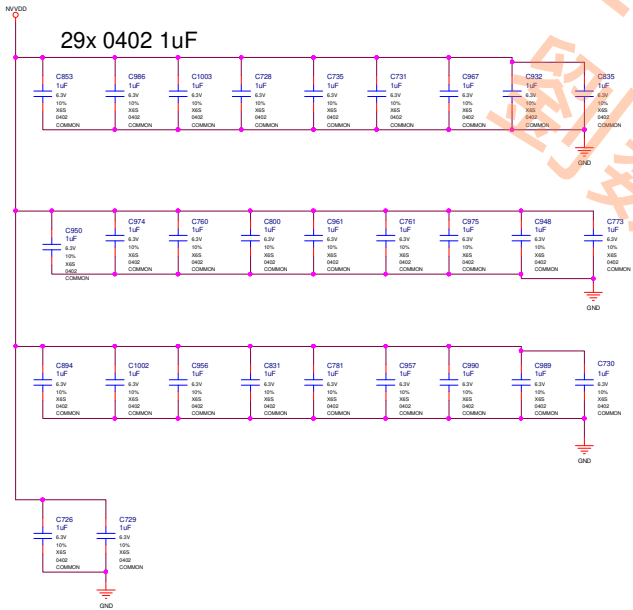
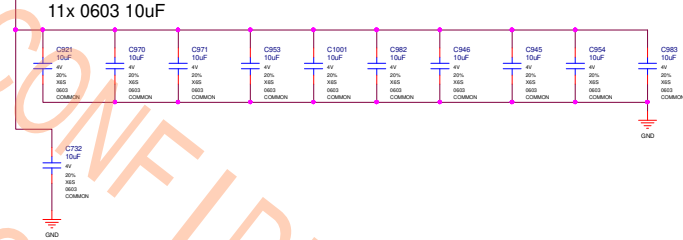
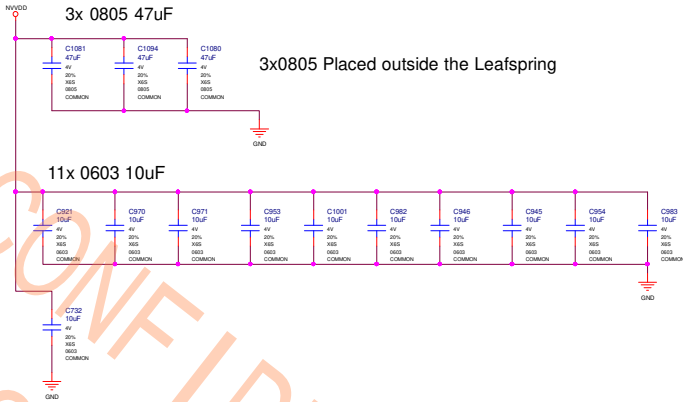
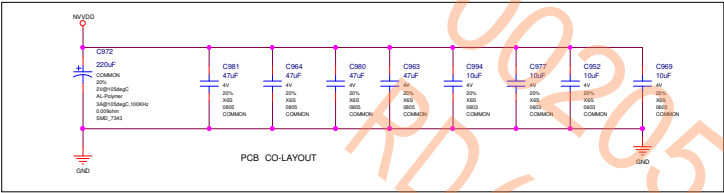
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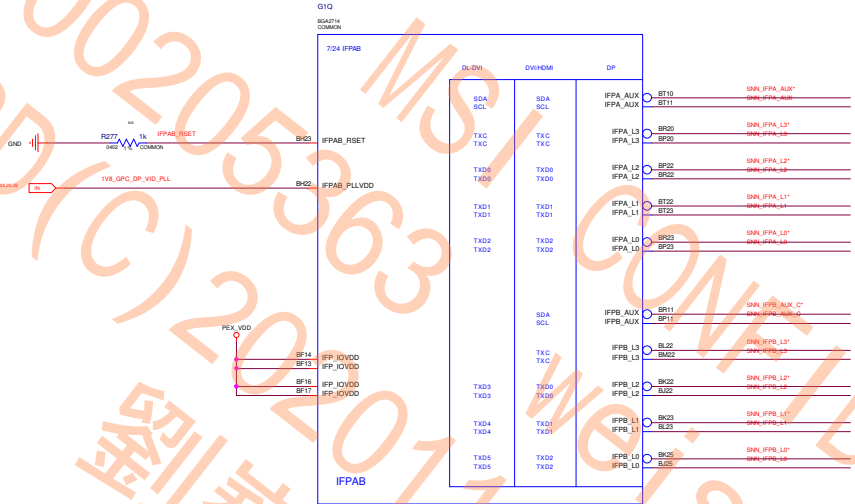


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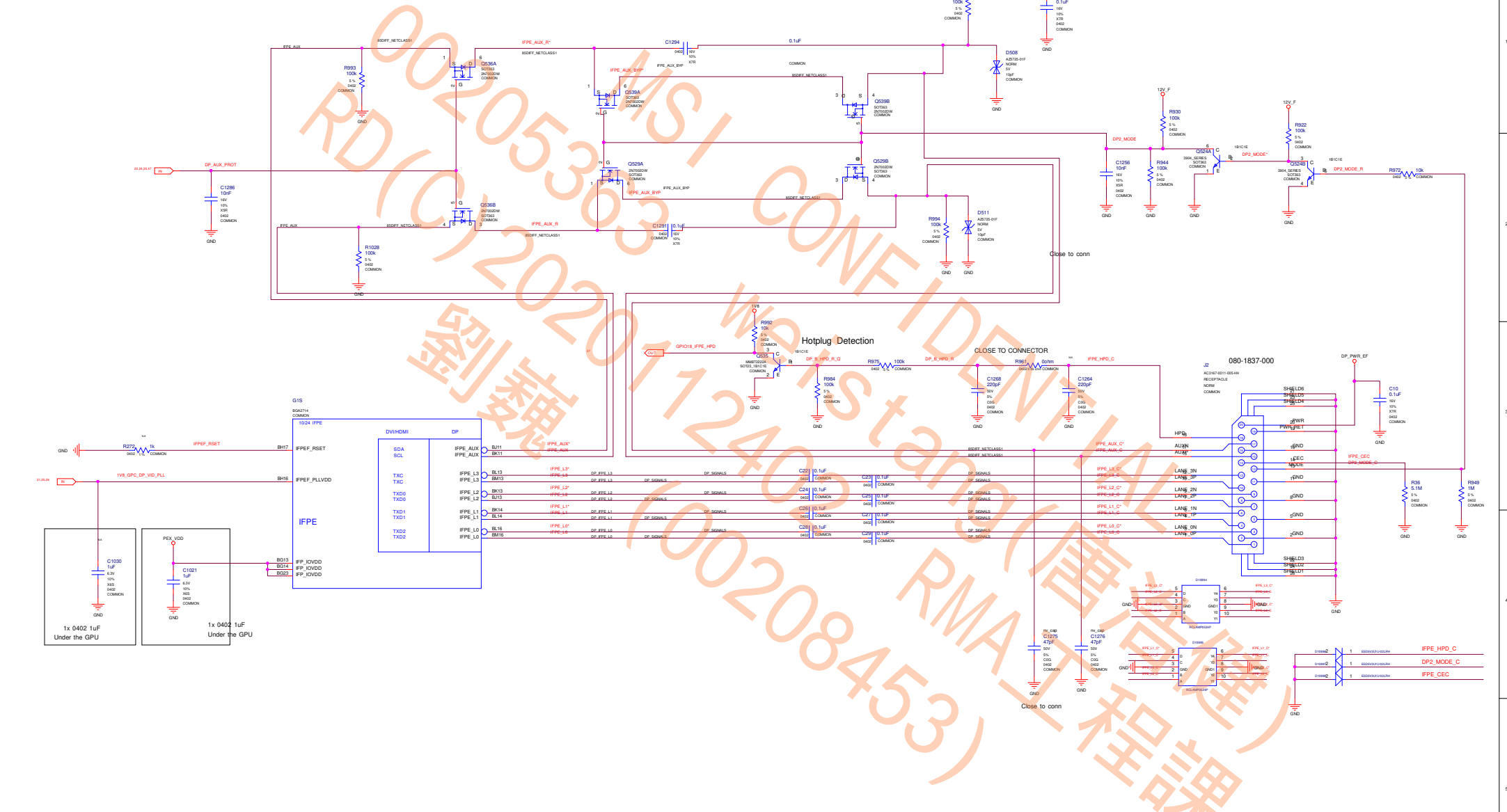


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STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG SAMSUNG 8Gb 7GHz
L	L	H	00001	RAMCFG MICRON 8Gb 7GHz
L	H	L	00010	RAMCFG HYNIX 8Gb 7GHz
H	H	L	00110	RAMCFG SAMSUNG 16Gb 8GHz
		TBD		

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M=Middle:Tied to 0.9V
L=Low :Tied to 0V

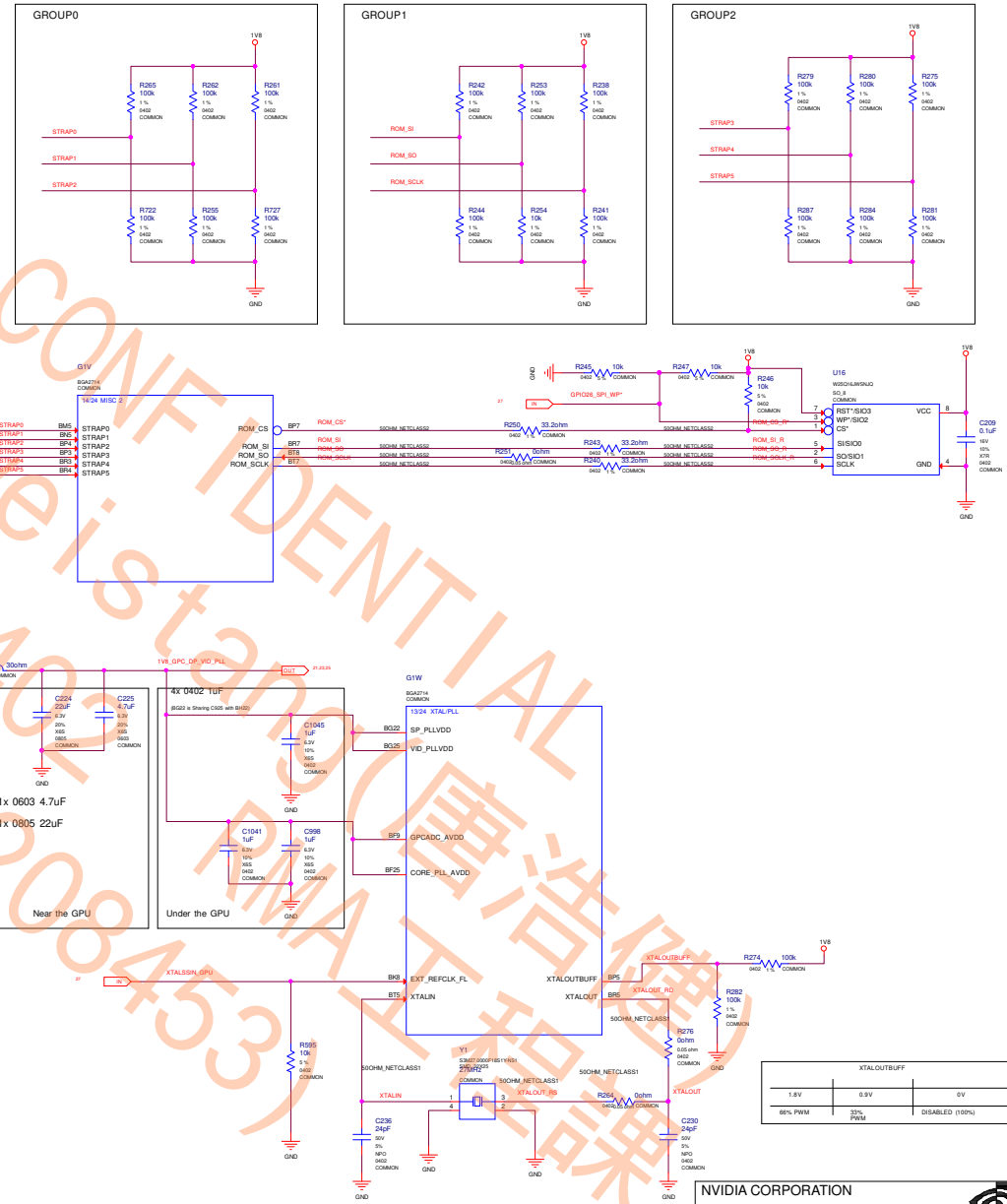
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H	H	M	0000	FS_OVERT DISABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
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H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



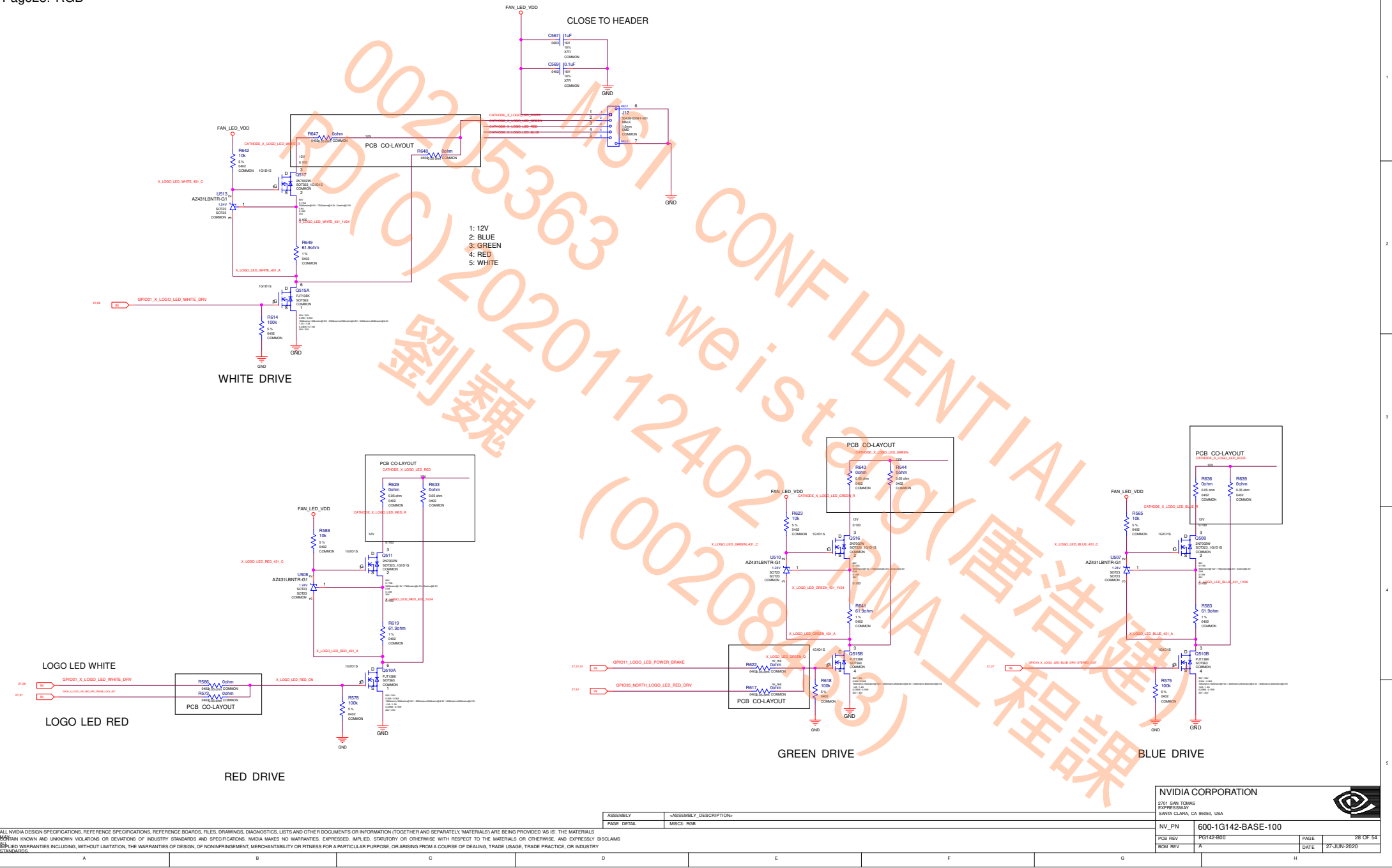
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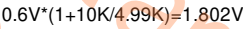
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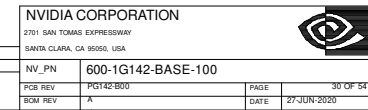




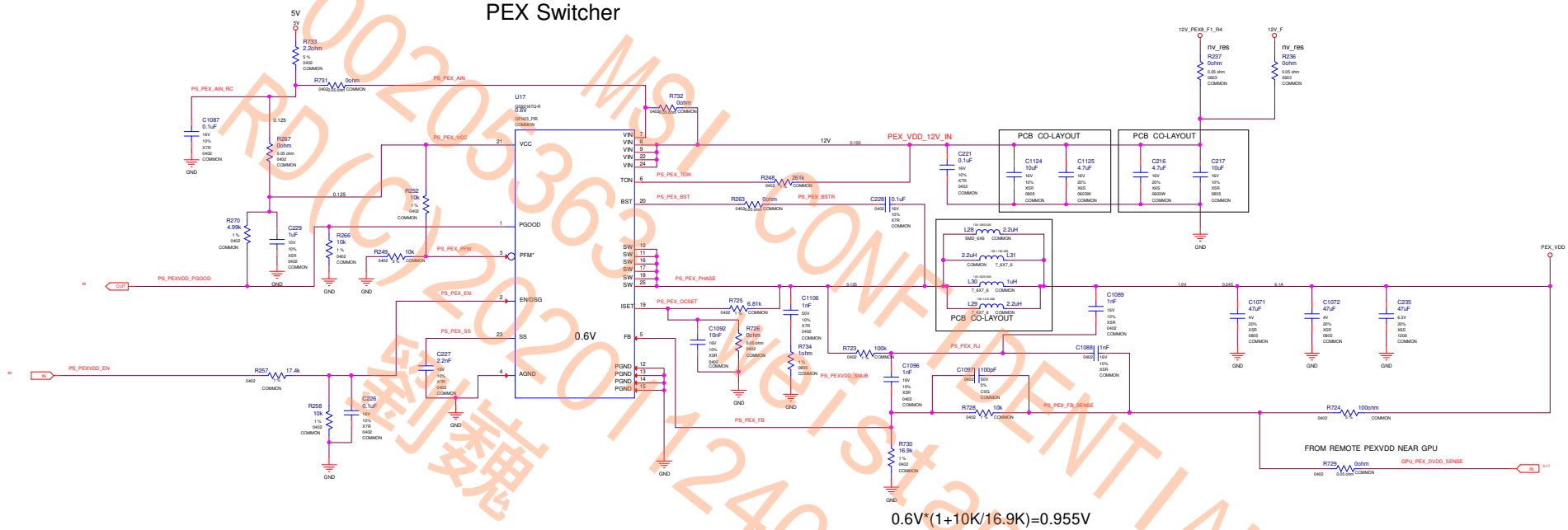
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PEX Switcher



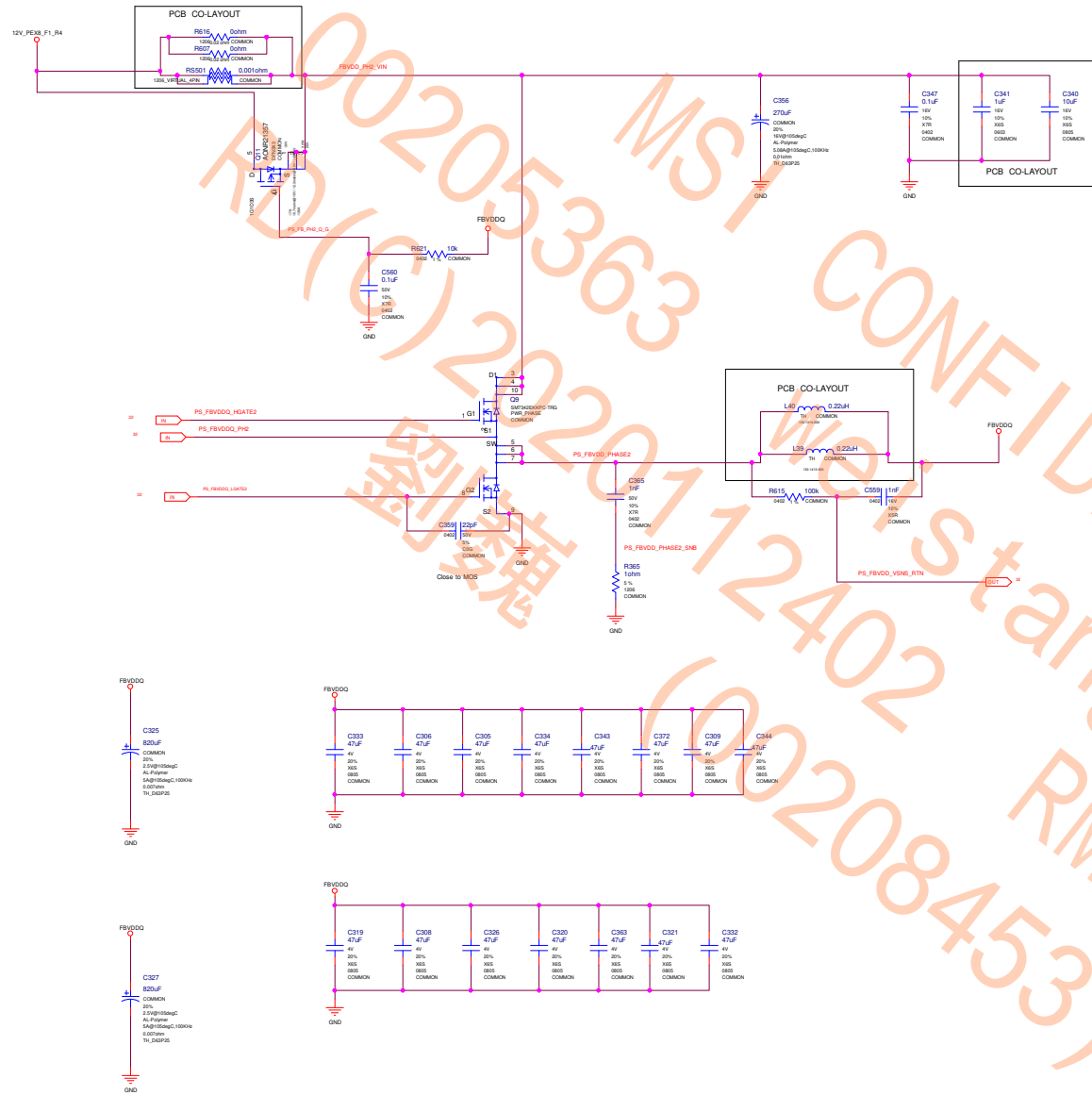
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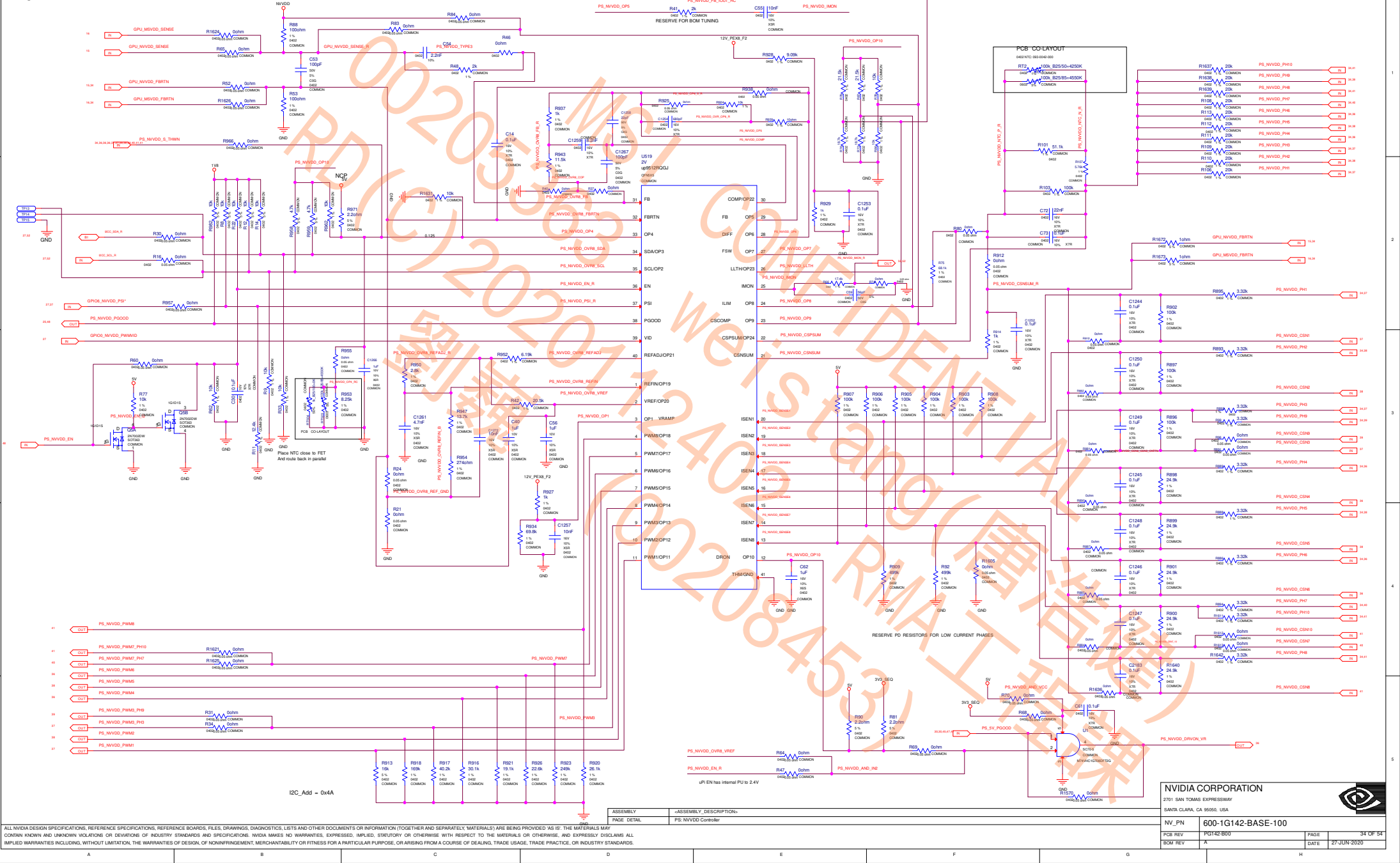
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FBVDD PH2 INPUT ANTI-BACKDRIVE



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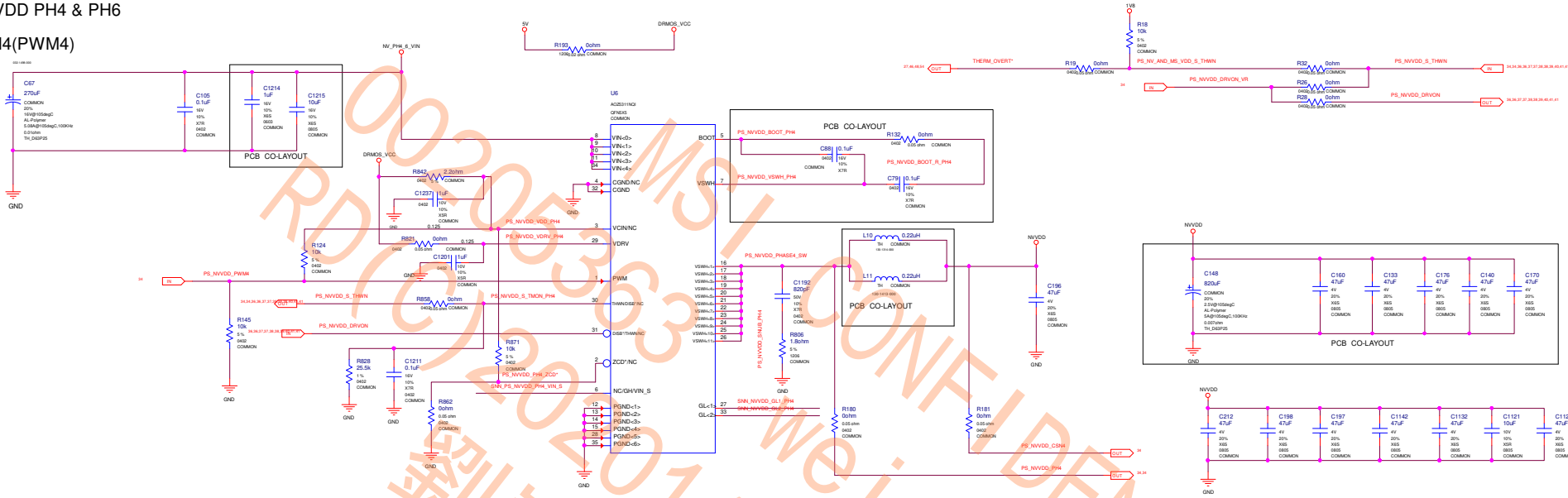
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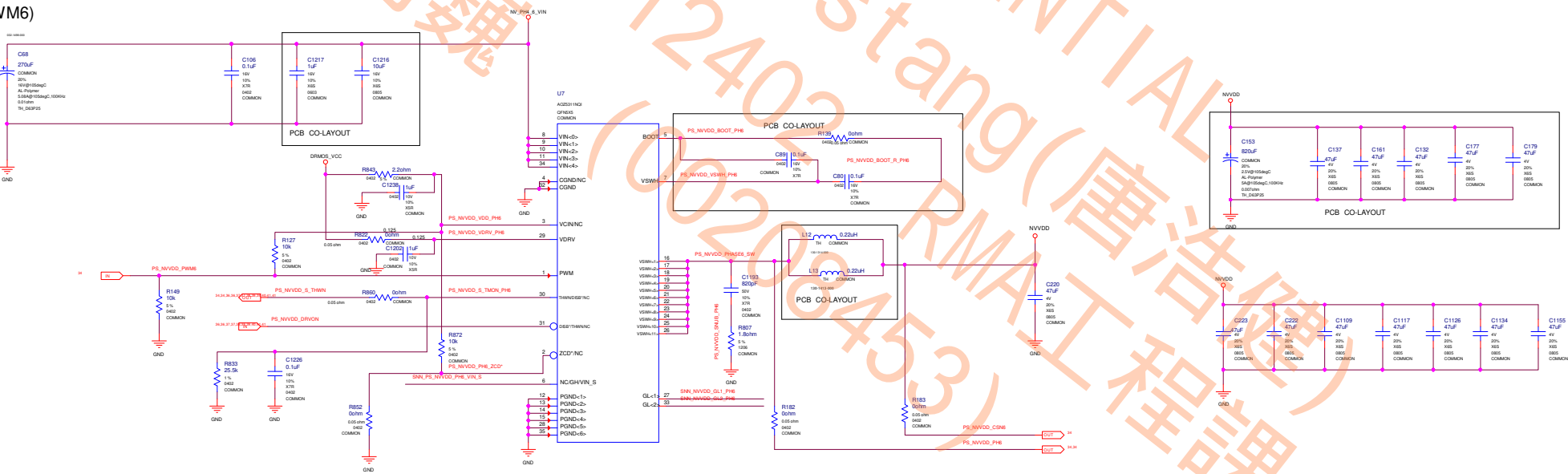
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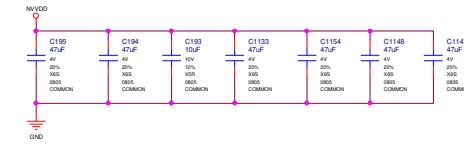
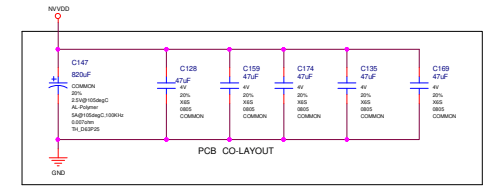
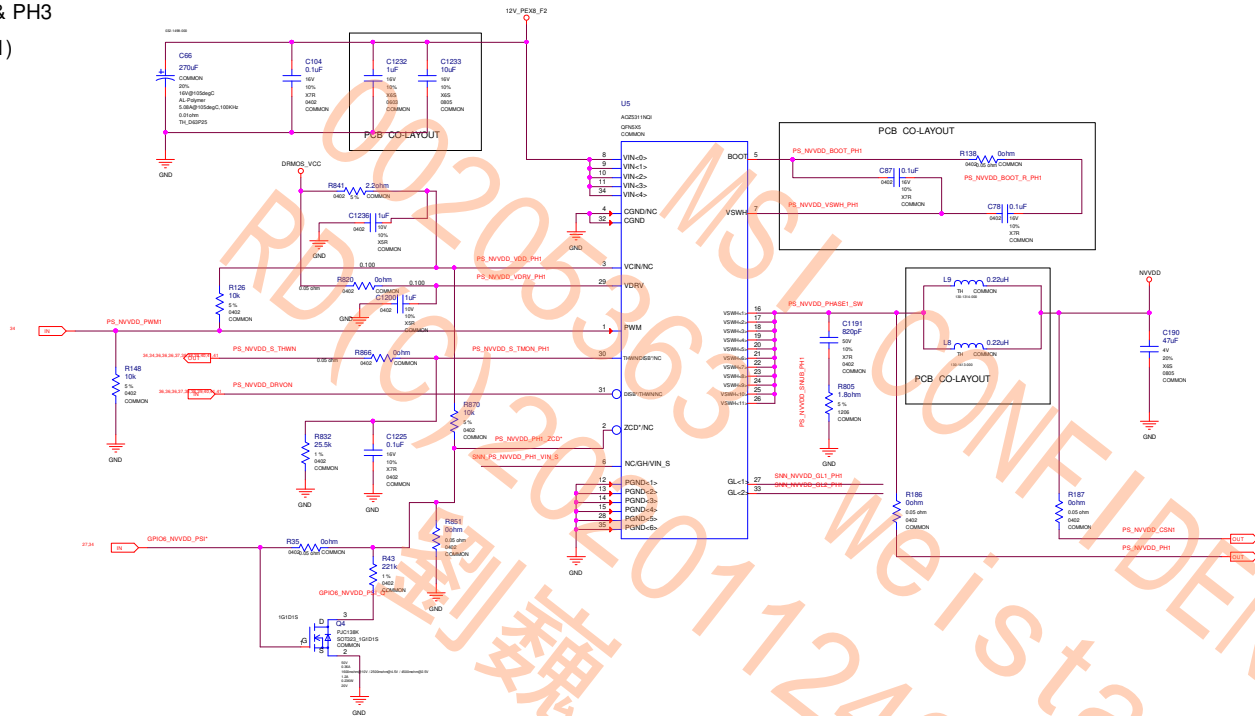


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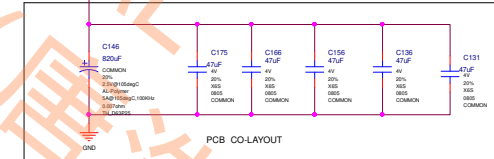
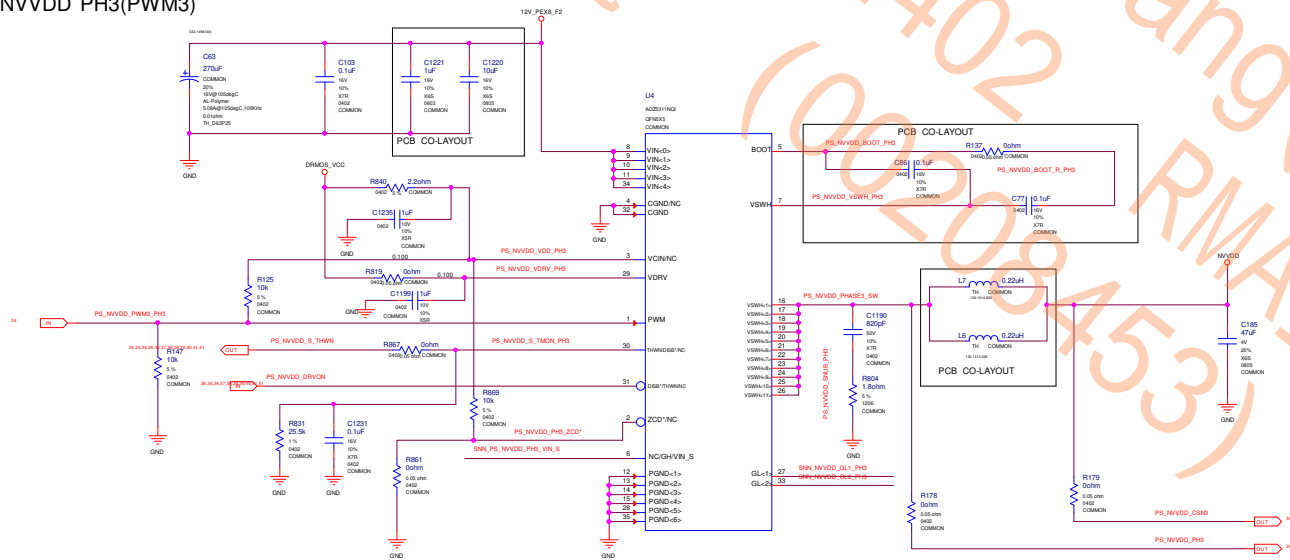


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NVVDD PH1(PWM1)



NVVDD PH3(PWM3)



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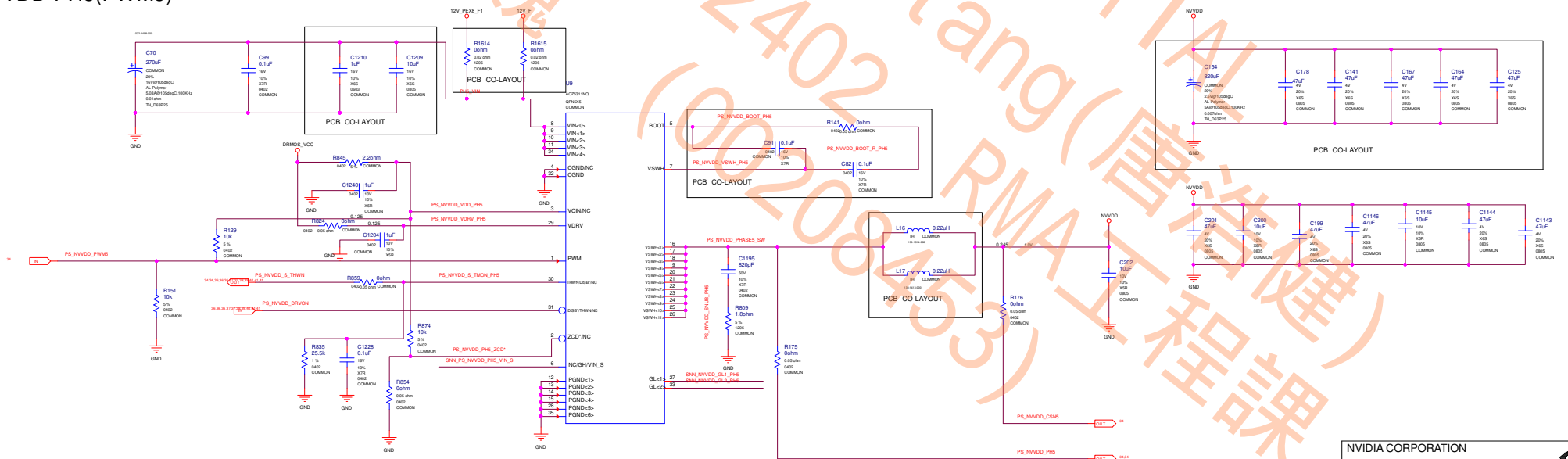
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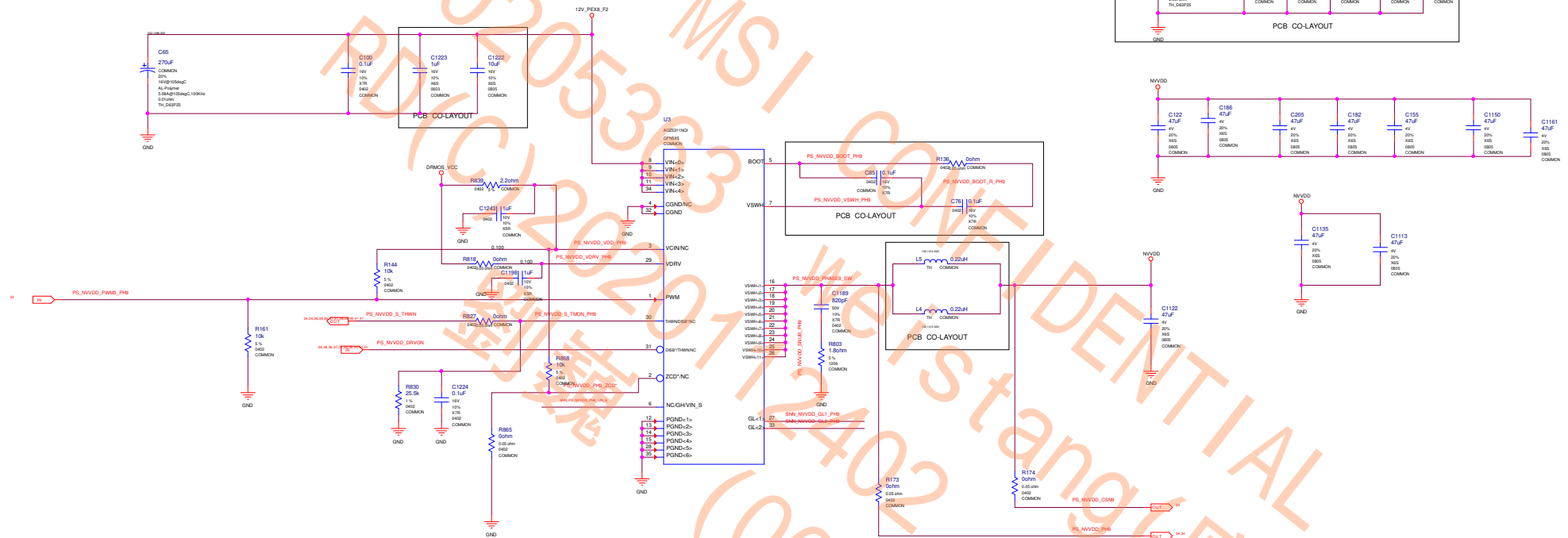
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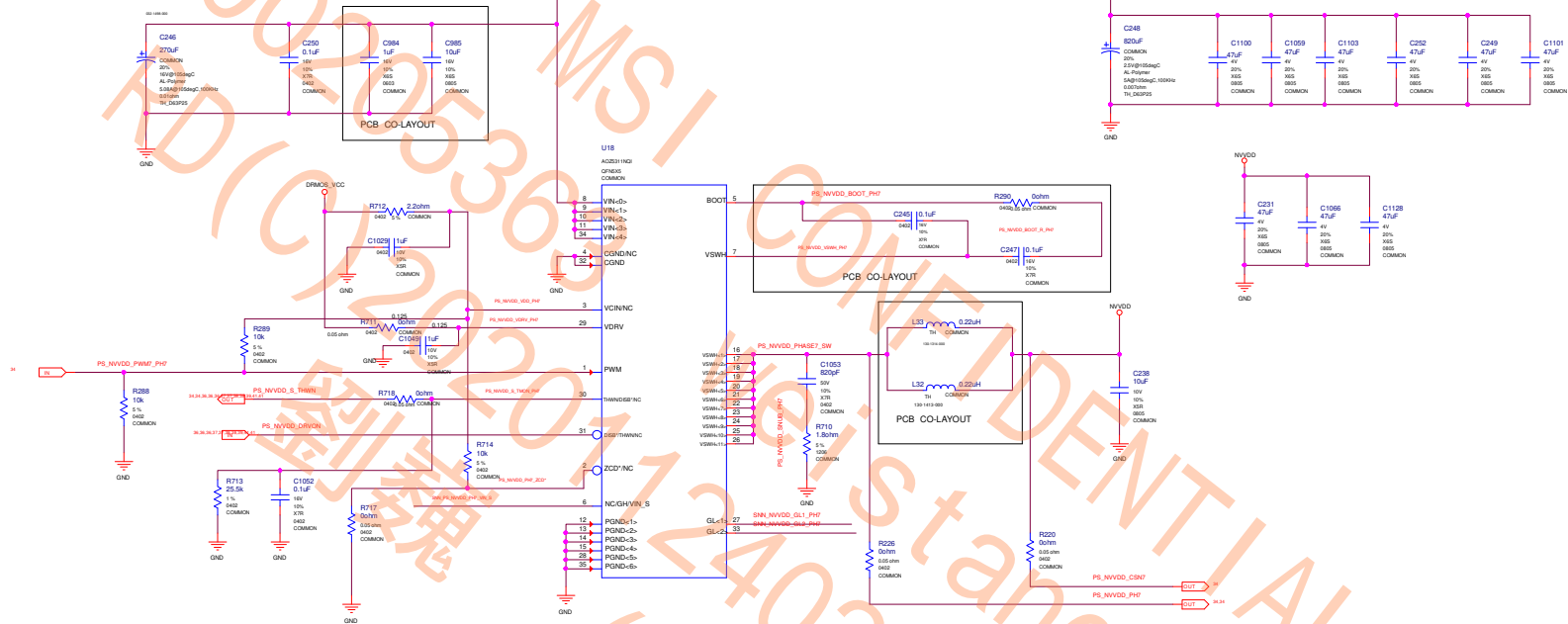
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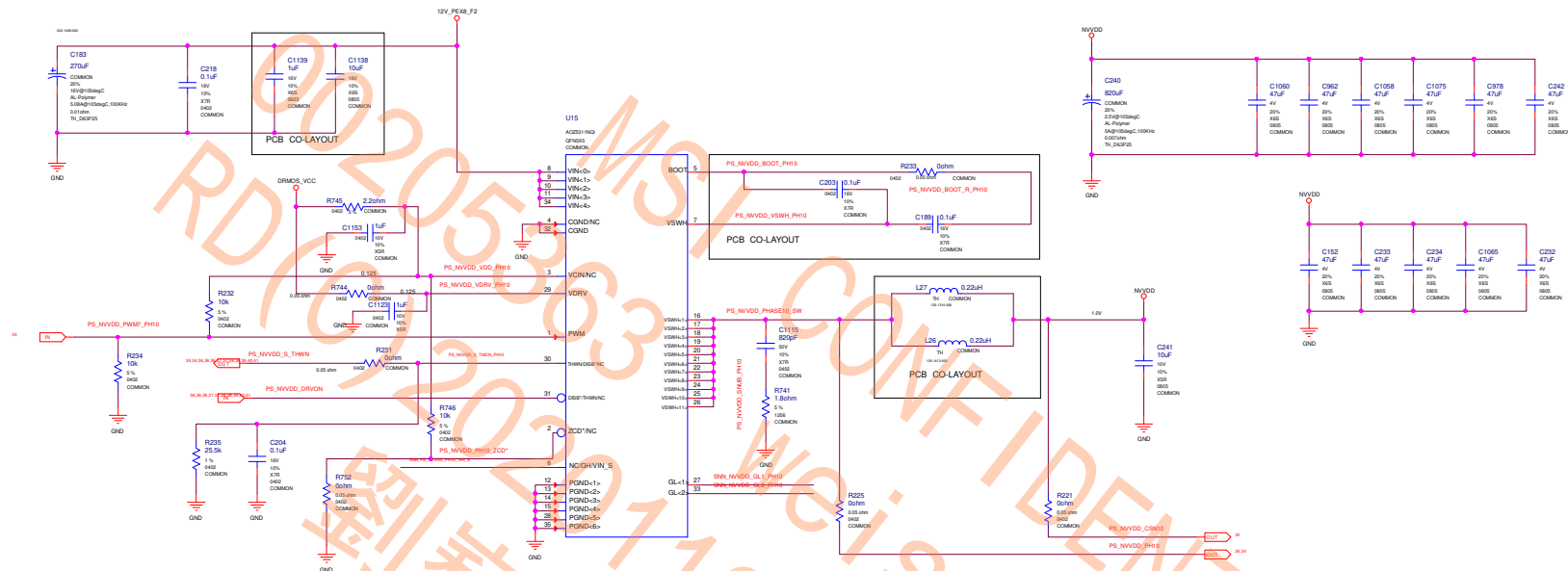


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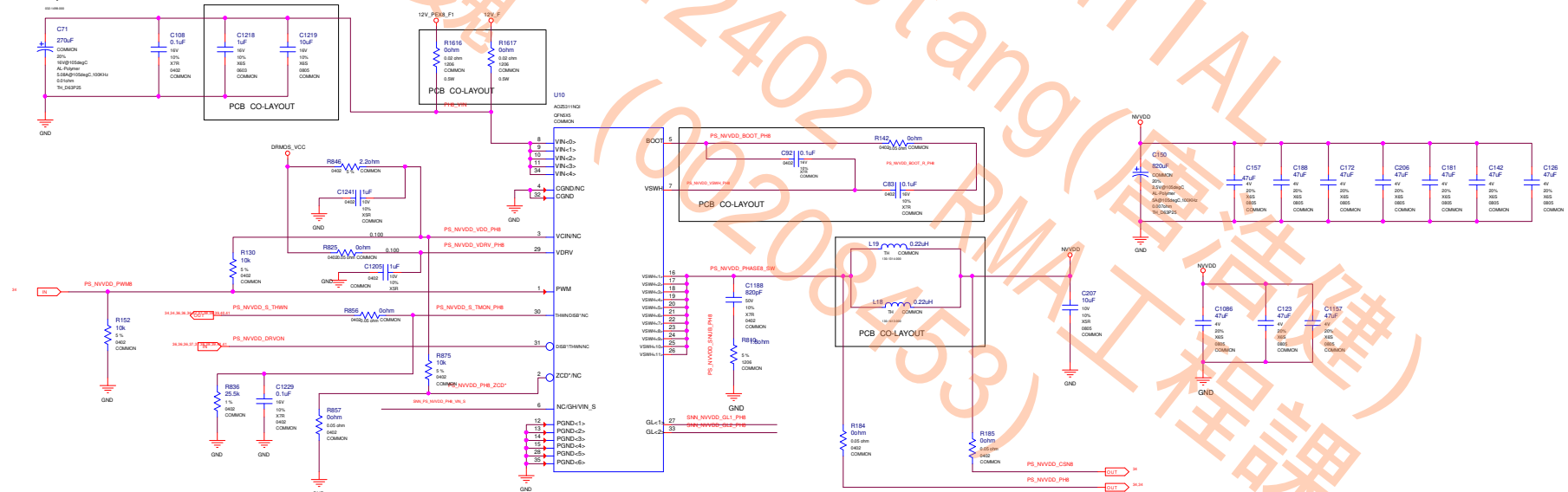
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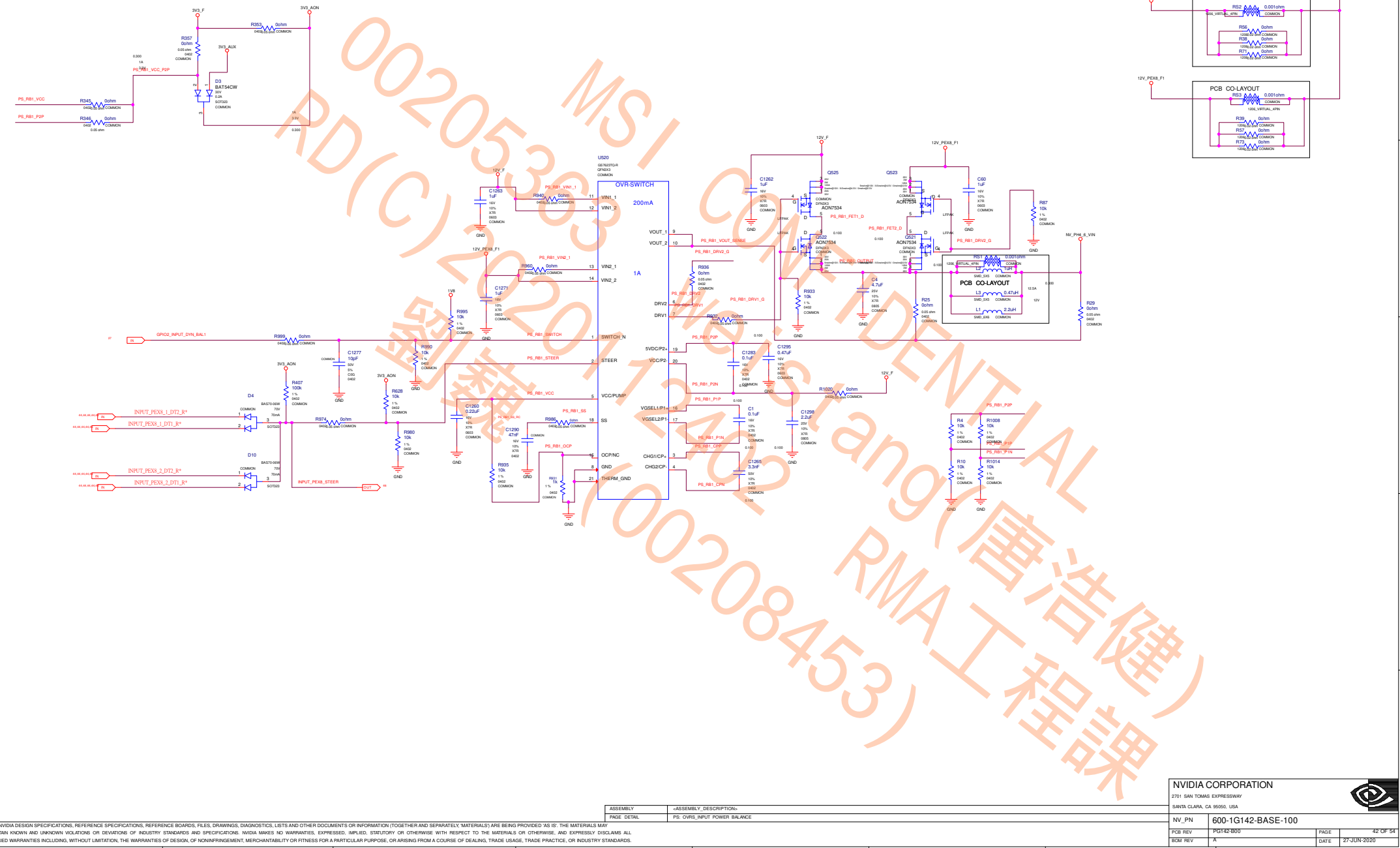
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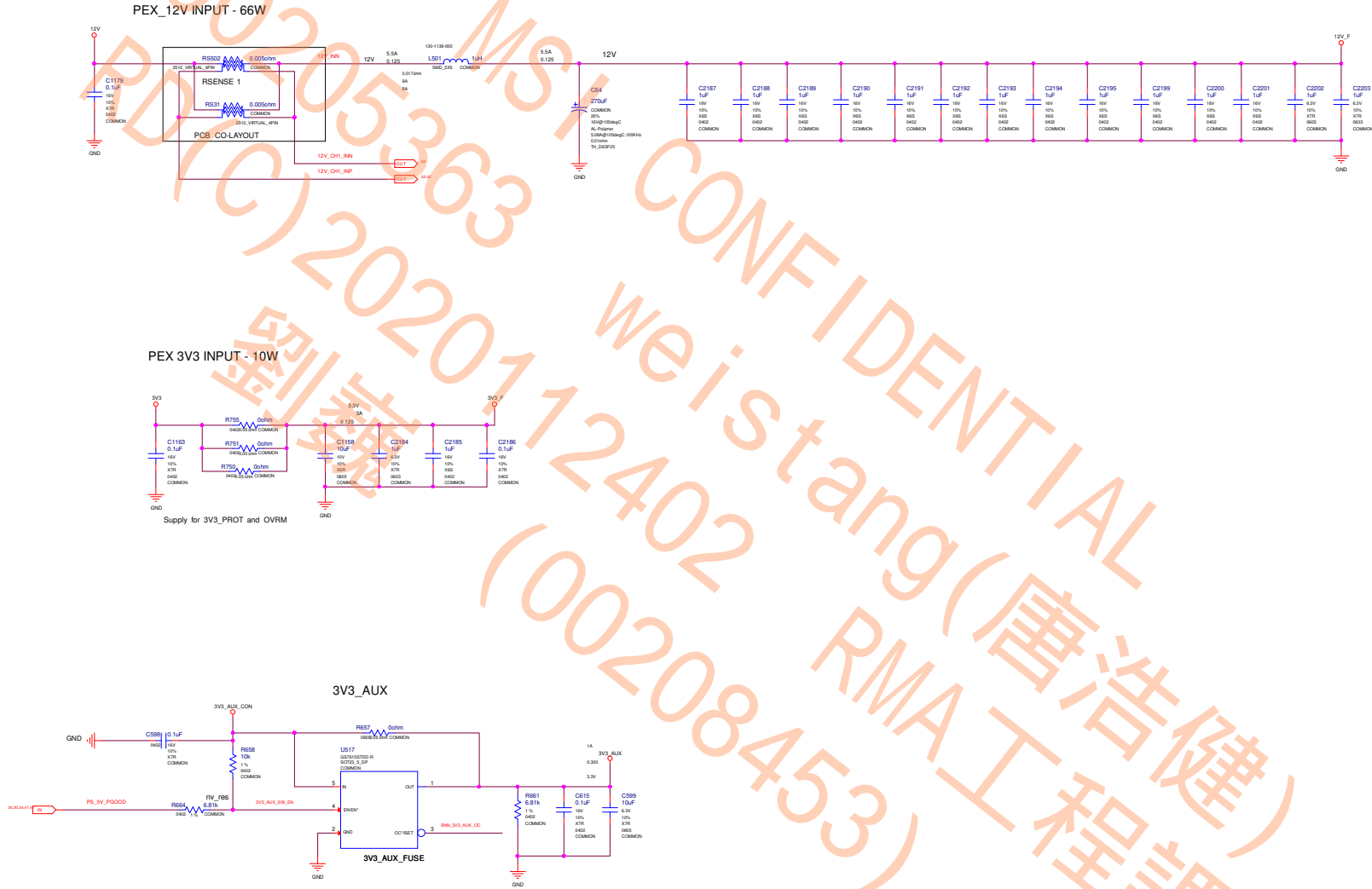
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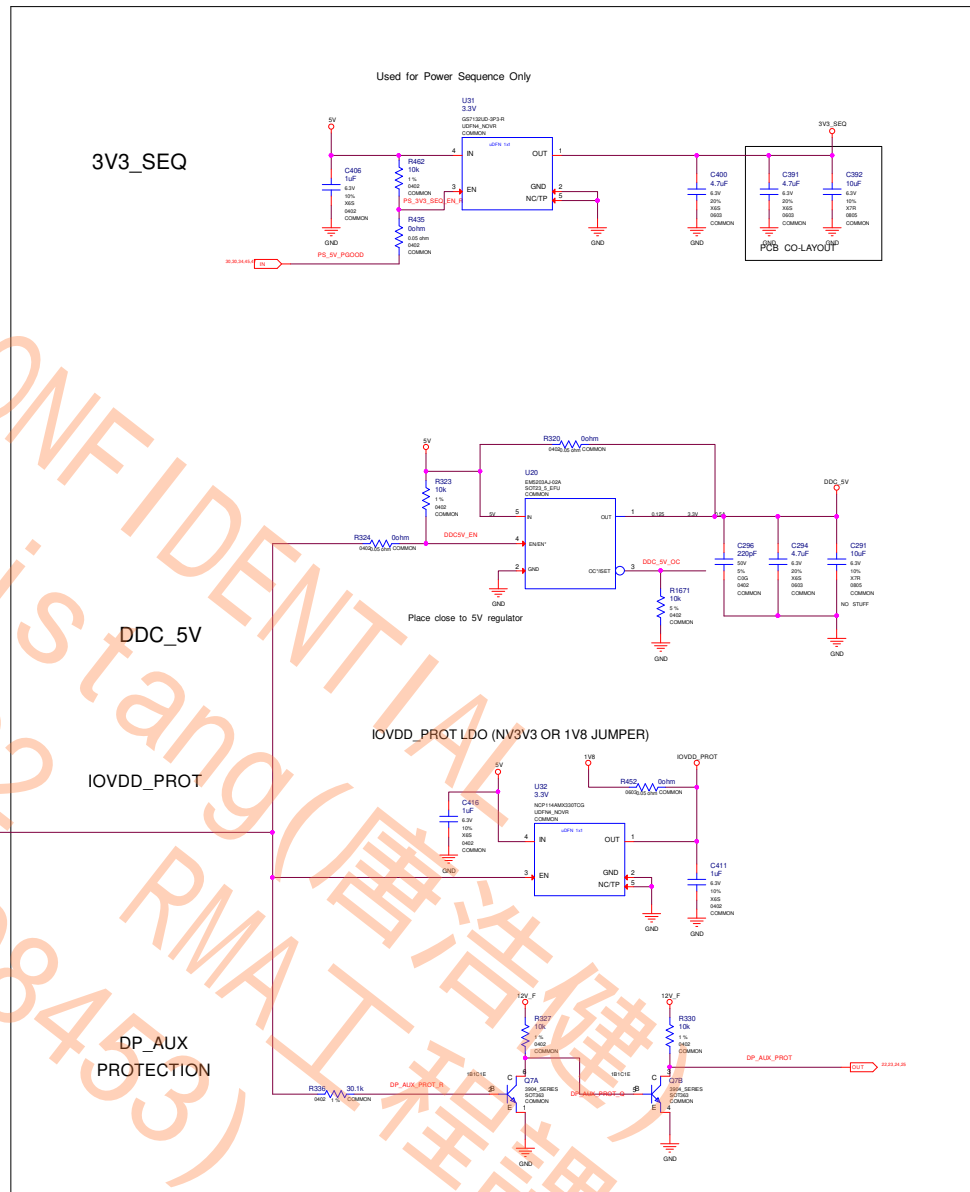
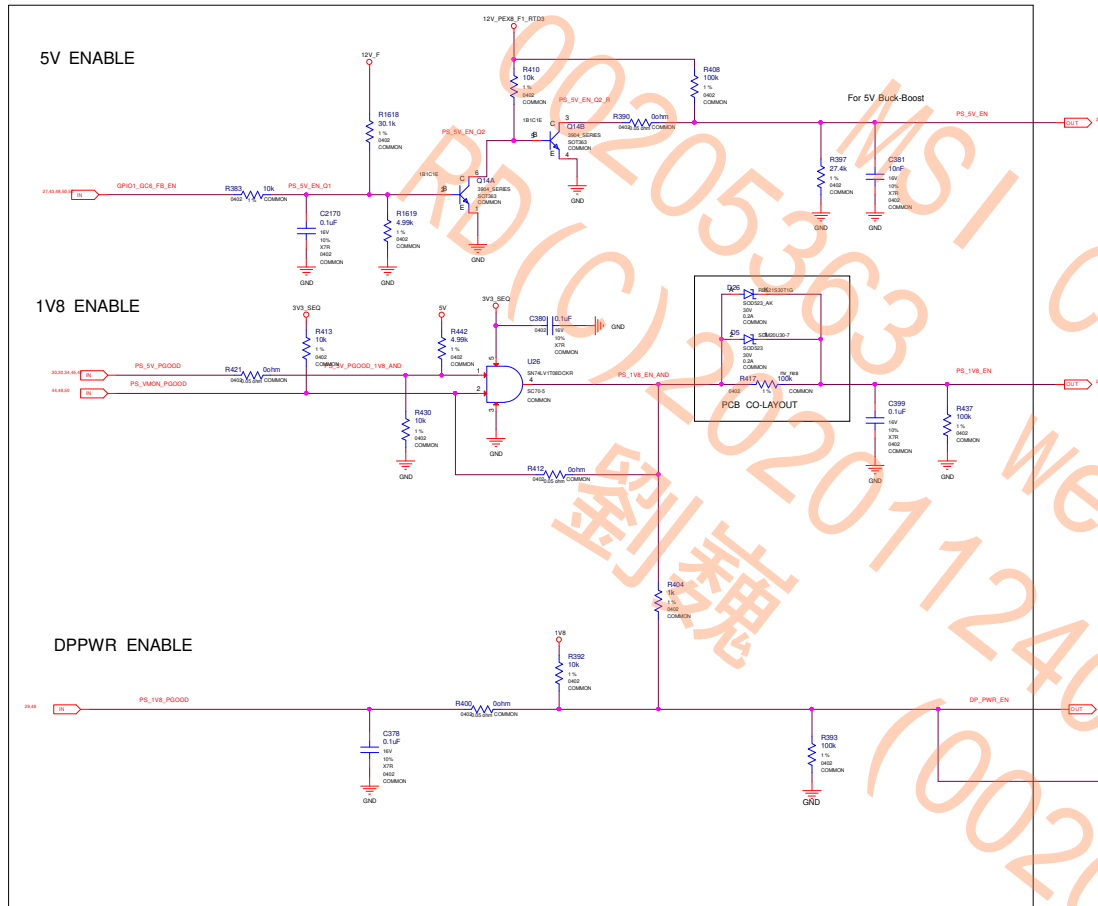
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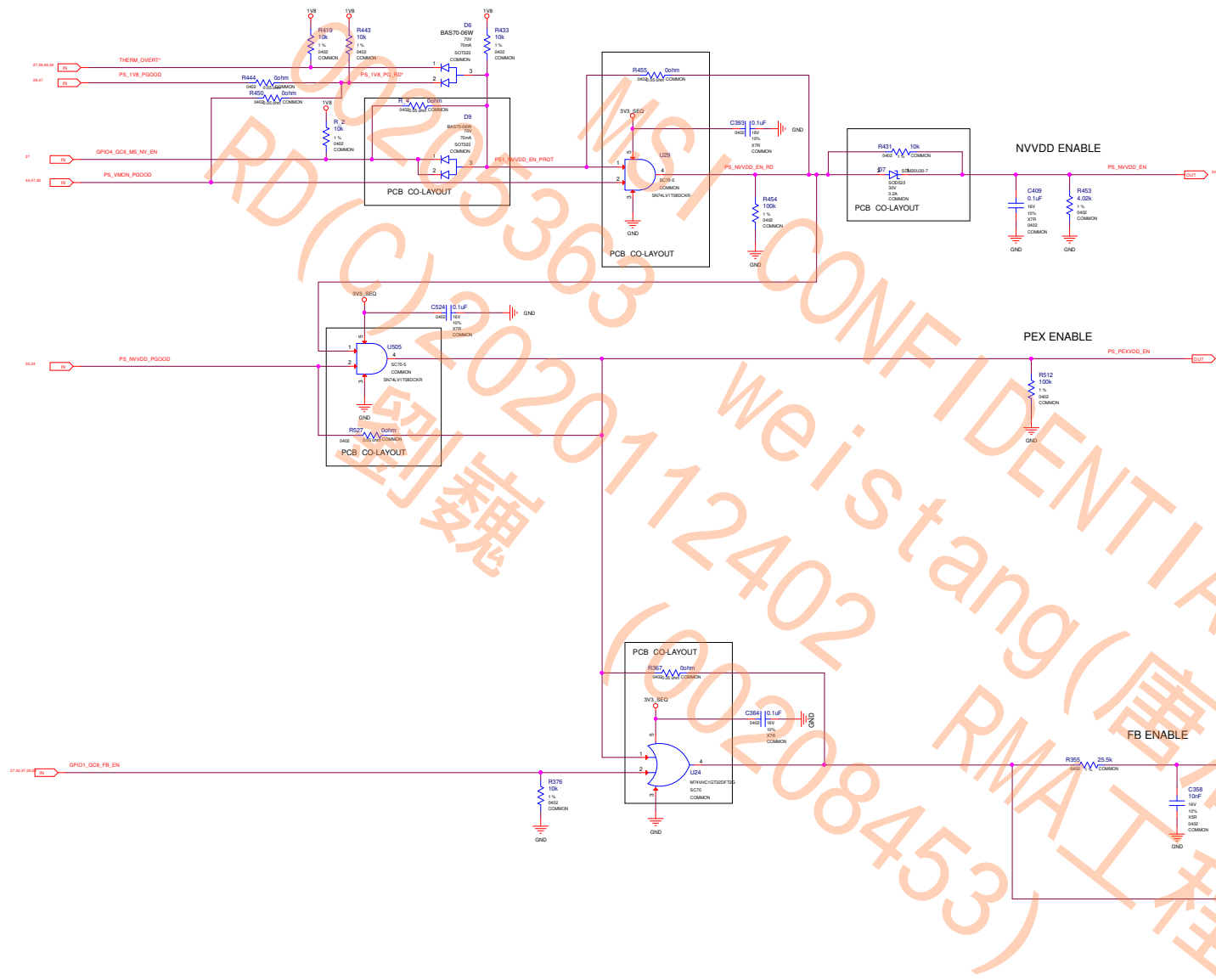
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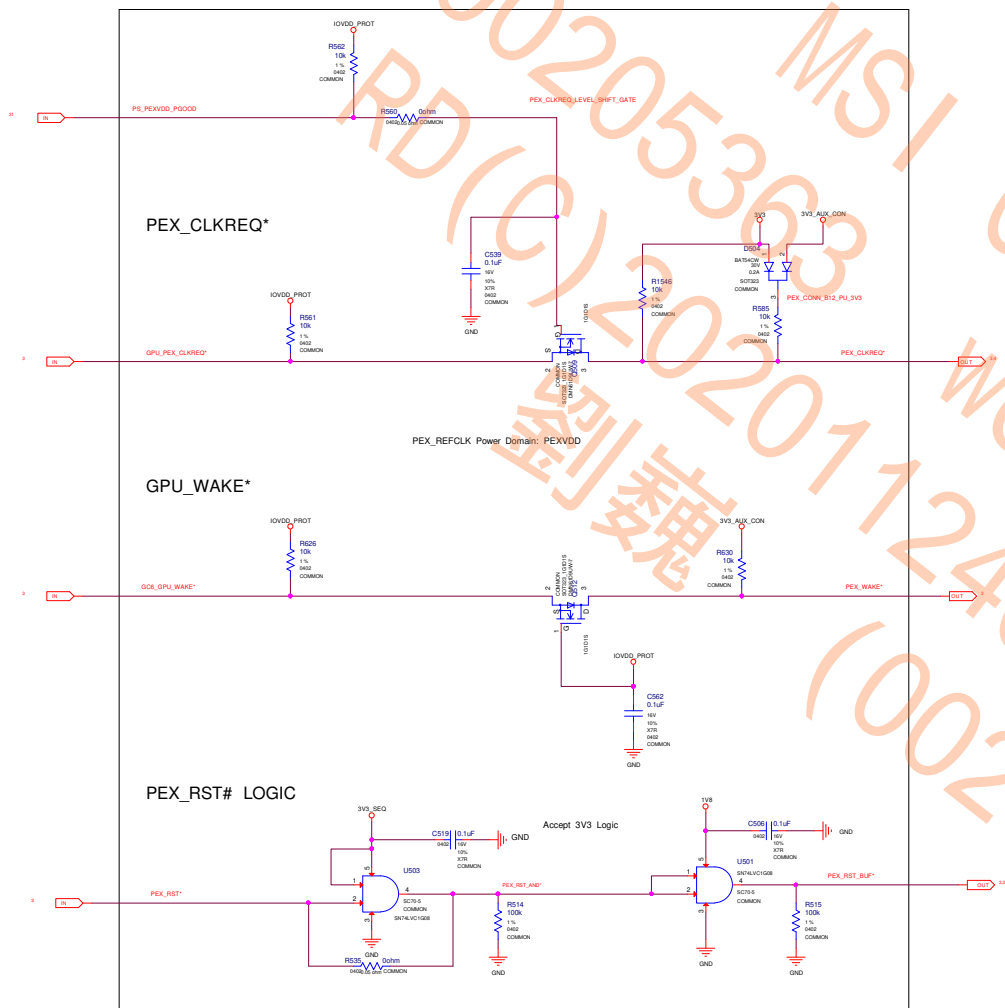


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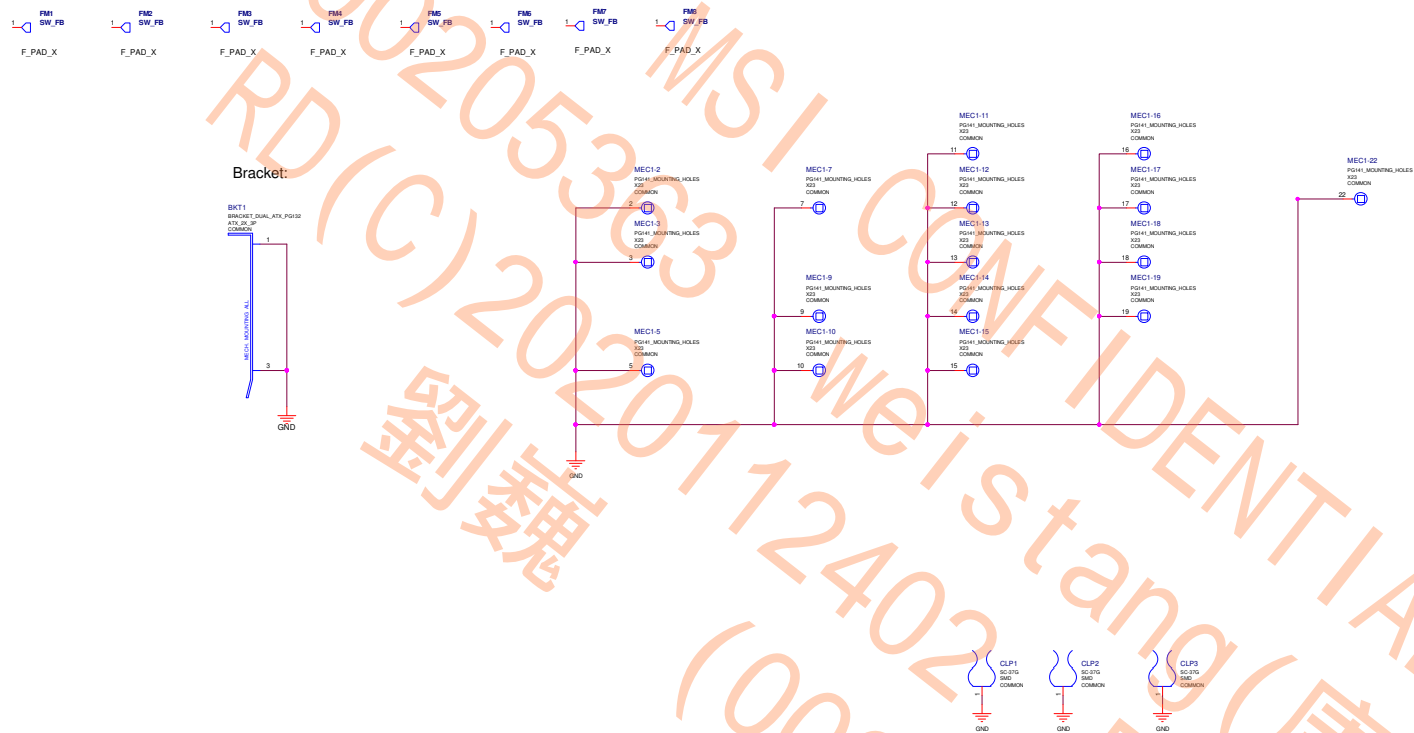
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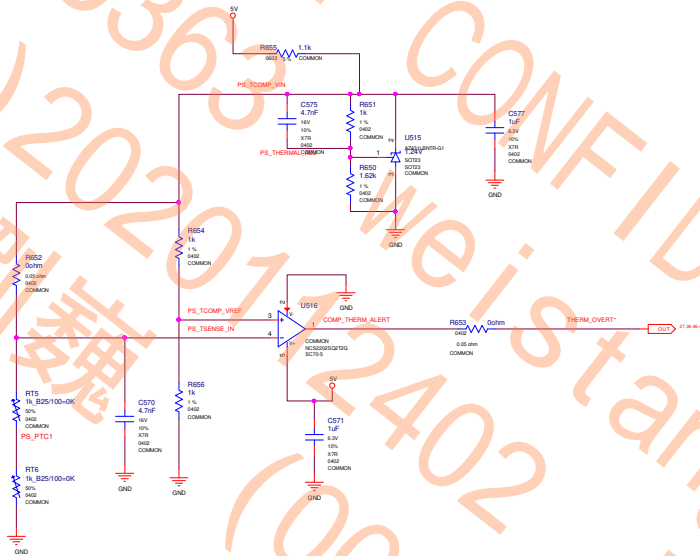


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